Data Sheet

VT6315N
PCI Express 1394a-2000 Integrated Host Controller

November 14, 2008

Preliminary Revision 1.0

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1 Product Features

VT6315N
PCI Express 1394a-2000 Integrated Host Controller

- **PCI Bus and Basic Function Specification**
  - Complies with PCI Express Rev 1.1
  - Supports Advanced Error Reporting capability
  - Active State Power Management (ASPM) to L0s and L1
  - Flexible programmable Bus master burst sizes and advanced internal arbitration control to optimize the bus utilization
  - Compliant with PCI bus power management specification V1.2
  - Supports I^2C EEPROM
  - EEPROM contains other hardware configuration
  - Supports Shadow EEPROM mechanism for EEPROM-less application

- **1394 Function Specification**
  - Single chip compliance with IEEE 1394a-2000, 1394-1995 and 1394a Open HCI host controller integrated 2-port PHY layer function
  - Compliance with 1394 Open HCI specification 1.0 and 1.1
  - Compliance with IEEE 1394-1995 specification release 1.0
  - Compliance with IEEE 1394a-2000
  - Provides 8 isochronous transmit contexts
  - Provides 4 isochronous receive contexts
  - Supports 400 / 200 / 100 Mbps of data transfer rate
  - General DMA controller control mechanism and I/F design
  - 3-deep physical post write queue
  - 4-deep physical response queue
  - GUID PROM shadow to EEPROM

- **Power and Clock Specification**
  - Supports CLKREQ# to enhance power management for mobile PC
  - Operates at 3.3V power supply
  - Built-in 3.3V to 1.2V regulator
  - 2 kV ESD protection
  - Crystal oscillator: 24.576 MHz for 1394

- **Package Type**
  - QFN-48 package (7 mm x 7 mm)

2 Overview

VT6315N is a highly integrated controller with PCI-Express x1 interface which integrates IEEE 1394a-2000 OHCI link layer controller with integrated 400 Mbps 2 ports 1394a PHY. VT6315N's 1394 OHCI Host Controller provides high performance serial connectivity. It implements the Link and Phy layers for IEEE 1394-1995 High Performance Serial Bus specification and 1394a-2000. It is compliant with 1394 OHCI Rev. 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCI host bus interface.

VT6315N is ready to provide industry-standard IEEE 1394 peripheral connections and it can support 100, 200 and 400 Mbit/s transmission via an integrated PHY. VT6315N services two types of data packets: asynchronous and isochronous (real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations.

The 1394a function of VT6315N is supported by the Microsoft host driver, which is built in Windows 98 Second Edition, Windows ME, Windows 2000, Windows XP, Windows 2003 server, and Windows Vista.

VT6315N is designed for the motherboard, desktop PC, and embedded system platform that can implement it in a small physical space to provide a variety of 1394a functions.

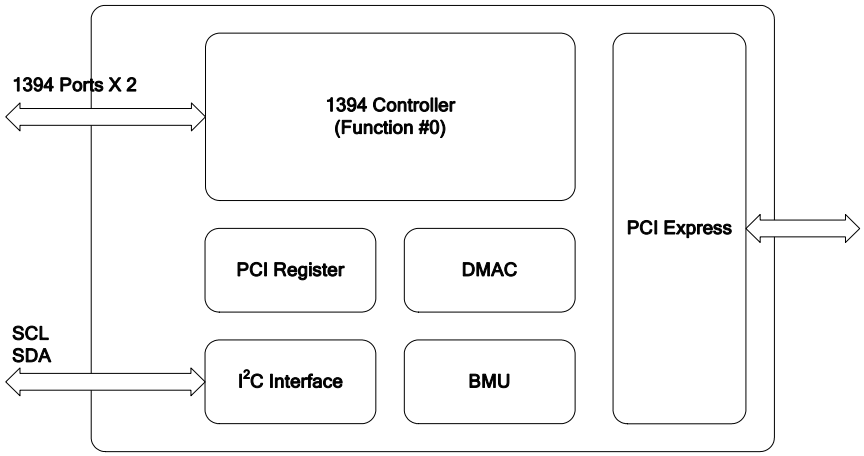


Figure 1 – VT6315N Block Diagram

3 Pinout

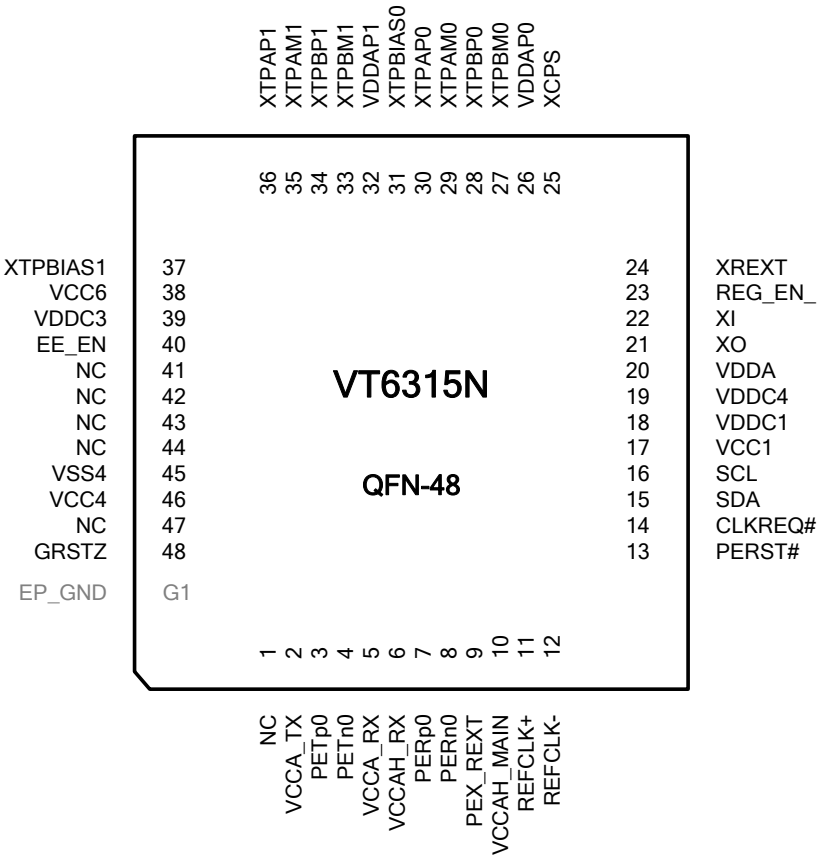


Figure 2 – VT6315N Pin Diagram for QFN-48 (Top View)

4 Pin List

Table 1 – VT6315N Pin List

Pin	Pin Name	Pin	Pin Name
14	CLKREQ#	20	VDDA
40	EE_EN	26	VDDAP0
48	GRSTZ	32	VDDAP1
4	PETn0	18	VDDC1
3	PETp0	39	VDDC3
8	PERn0	19	VDDC4
7	PERp0	45	VSS4
13	PERST#	25	XCPS
9	PEX_REXT	22	XI
11	REFCLK+	21	XO
12	REFCLK-	24	XREXT
23	REG_EN_	29	XTPAM0
16	SCL	35	XTPAM1
15	SDA	30	XTPAP0
17	VCC1	36	XTPAP1
46	VCC4	31	XTPBIAS0
38	VCC6	37	XTPBIAS1
5	VCCA_RX	27	XTPBM0
2	VCCA_TX	33	XTPBM1
10	VCCAH_MAIN	28	XTPBP0
6	VCCAH_RX	34	XTPBP1
G1	EP_GND		

5 Pin Description

Table 2 – Signal Type Definitions

Type	Description
I	**Input.** Standard input-only signal.
O	**Output.** Standard active output driver.
I/O	**Input/output.** An input/output signal.
T/S	**Tri-state.** Inactive bi-directional input/output pin.
OD	**Open drain.** Allows multiple devices to share as a wire-OR.
A_{DIFF}	**Analog differential.** Signal pair for the twisted-pair interface.
A_{BIAS}	**Analog bias or reference signal.** Must be tied to external resistor and/or capacitor bias network, as shown in the system schematic.

PCI Express Interface

Pin Name	Pin #	I/O	Signal Description
PETp0, PETn0	3, 4	A_{DIFF}	PCI Express Transmitter Differential Pair
PERp0, PERn0	7, 8	A_{DIFF}	PCI Express Receiver Differential Pair
REFCLK+, REFCLK-	11, 12	I	PCI Express Differential Clock The PCI Express externally provides differential clock with 100Mhz ±300ppm. Spread Spectrum Clocking (SSC) is allowed
PEX_REXT	9	A_{BIAS}	Bias pin to external 5.6 kΩ (±1%) resistor tied to analog ground.
PERST#	13	I	PCI Express Reset When PERST# is asserted low, the chip performs an internal system hardware reset. PERST# may be asynchronous to PCICLK asserted or deasserted. It is recommended that the deassertion be synchronous to guarantee clean and bounce free edge. The PERST# assertion/deassertion should meet the timing spec defined in PCI Express Card Electromechanical Specification Revision 1.1a.
CLKREQ#	14	OD	Clock Request When CLKREQ# is disabled, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked clock state. The CLKREQ# assertion/ deassertion is asynchronous to reference clock and should meet the timing spec defined in PCI Express Card Electromechanical Specification Revision 1.1.

I^2C Interface

Pin Name	Pin #	I/O	Signal Description
SCL	16	IO	Serial Clock
SDA	15	IO	Serial Data

1394 PHY Interface

Pin Name	Pin #	I/O	Signal Description
XTPAP0, XTPAM0	30, 29	A_{DIFF}	Twisted Pair Cable A Differential Signal Terminals. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, XTPAP0 and XTPAM0 can be left open.
XTPAP1, XTPAM1	36, 35	A_{DIFF}	Twisted Pair Cable A Differential Signal Terminals. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, XTPAP1 and XTPAM1 can be left open.
XTPBP0, XTPBM0	28, 27	A_{DIFF}	Twisted Pair Cable B Differential Signal Terminals. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, XTPBP0 and XTPBM0 can be left open.
XTPBP1, XTPBM1	34, 33	A_{DIFF}	Twisted Pair Cable B Differential Signal Terminals. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, XTPBP1 and XTPBM1 can be left open.
XTPBIAS0, XTPBIAS1	31, 37	O	Twisted Pair Bias Output This provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for signaling to the remote nodes that there is an active cable connection. Each of these pins must be decoupled with a 1.0 uF capacitor to ground. For unused port, XTPBIAS0 and XTPBIAS1 can be floating.
XI	22	I	Crystal Input This pin must be connected to a 24.576 MHz parallel resonant fundamental mode crystal.
XO	21	O	Crystal Output This pin must be connected to a 24.576 MHz parallel resonant fundamental mode crystal.
XCPS	25	I	Cable Power Status Input An internal comparator is used to detect the presence of cable power.
XREXT	24	I	External Resistor A 5.6 kΩ resistor is required for internal current source operation.

Miscellaneous

Pin Name	Pin #	I/O	Signal Description
EE_EN	40	I	I^2C EEPROM Enable Control This pin is connected to ground through a 4.7 kΩ resistor when Shadow EEPROM mechanism for EEPROM-less application is used. Otherwise leave it unconnected.
GRSTZ	48	I	Global Reset Input Connect an external capacitor (typically 1.0 μF) to guarantee that the reset will be delayed until after the supply voltage is completely stabilized. The input can be also driven by an open-drain output buffer.
REG_EN_	23	I	Internal Voltage Regulator Enable This pin must be connected to ground for normal operation.

Power and Ground

Pin Name	Pin #	I/O	Signal Description
VCC1, VCC4, VCC6	17, 46, 38	P	Chip Power 3.3V
VCCAH_MAIN, VCCAH_RX	10, 6	P	Chip Power 3.3V
VDDA, VDDAP0 VDDAP1,	20, 26, 32	P	Chip Power 3.3V
VSS4	45	P	Chip Ground
VDDC1, VDDC3, VDDC4	18, 39, 19	P	Core Power 1.2V
VCCA_TX, VCCA_RX	2, 5	P	Core Power 1.2V
EP_GND	G1	P	QFN Package Ground

6 Registers Overview

PCI Function Registers

Table 3 – PCI Express Register Map

Offset	Register Name	Default
PCI Configuration Space Header		
1-0	Vendor ID	1106h
3-2	Device ID	3403h
5-4	Command	0000h
7-6	Status	0210h
8	Revision ID	nnh
0B-9	Class Code	0C0010h
0C	Cache Line Size	00h
0D	Latency Timer	00h
0E	Header Type	80h
0F	Built In Self Test	00h
13-10	OHCI CSR Memory Mapped IO (MMIO) Base	0000 0000h
17-14	CSR IO Base Address	0000 0001h
2B-18	RESERVED	-
2D-2C	Subsystem Vendor ID	1106h
2F-2E	Subsystem ID	3403h
30-33	RESERVED	-
34	Capability Pointer	50h
3B-34	RESERVED	-
3C	Interrupt Line	00h
3D	Interrupt Pin	01h
3E	Minimum Grant	00h
3F	Maximum Latency	20h
4F-40h	RESERVED	00h
Power Management		
50	Power Management Capabilities ID	01h
51	Next Pointer	00h
53-52	Power Management Capabilities	E403h
55-54	Power Management Control / Status	0000h
7F-56	RESERVED	-
MSI		
83-80	MSI Control Register Structure	0180 0005h
87-84	MSI Low Address	0000 0000h
8B-88	MSI High Address	0000 0000h
8F-8C	MSI Data Register	0000 0000h

Offset	Register Name	Default
93-90	MSI Mask	0000 0000h
97-94	MSI Pending	0000 0000h
PCI Express Capability Structure		
9B-98	PCI Express Capability	0011 C010h
9F-9C	Device Capability	0000 80C0h
A1-A0	Device Control	0000h
A3-A2	Device Status	0010h
A7-A4	Link Capability	0004 CC11h
A9-A8	Link Control	0000h
AB-AA	Link Status	1011h
Advance Error Reporting		
101-100	PCI Express Extended Capability ID	0001h
103-102	Next Pointer / Capability Version	1301h
107-104	Uncorrectable Error Status	0000 0000h
10B-108	Uncorrectable Error Mask	0000 0030h
10F-10C	Uncorrectable Error Severity	0006 2031h
113-110	Correctable Error Status	0000 0000h
117-114	Correctable Error Mask	0000 2000h
11B-118	Advanced Error Capability and Control	0000 00A0h
12B-11C	Header Log Registers	0h
Device Serial Number		
133-130	Device Serial Number Enhanced Capability	0001 0003h
137-134	Device Serial Number - Lower	0000 0000h
13B-138	Device Serial Number - Upper	0000 1106h

Memory-Space Registers

Table 4 – 1394 OHCI-Link Memory Space

Offset	Register Name	Default
3-0	Version (OHCI 1.0 Mode)	0001 0000h
	Version (OHCI 1.1 Mode)	0001 0010h
4	RESERVED (GUID ROM)	0000 0000h
0B-8	Asynchronous Transmit Retries	0000 0000h
0F-0C	CSR Data	0000 0000h
13-10	CSR Compare Data	0000 0000h
17-14	CSR Control	8000 0000h
1B-18	Configuration ROM Header	0000 0000h
1F-1C	1394 Bus ID	3133 3934h
23-20	1394 Bus Options	F000 0002h
27-24	Global Unique ID High	0000 0000h
2B-28	Global Unique ID Low	0000 0000h
33-2C	RESERVED	-
37-34	Configuration ROM Map	0000 0000h
3B-38	Posted Write Address Low	0000 0000h
3F-3C	Posted Write Address High	0000 0000h
43-40	Vendor ID	0000 0000h
4F-44	RESERVED	-
53-50	HC Control Set	0000 0000h
57-54	HC Control Clear	0000 0000h
5F-58	RESERVED	-
63-60	RESERVED	-
67-64	Self-ID Buffer Pointer	0000 0000h
6B-68	Self-ID Count	0000 0000h
6F-6C	RESERVED	-
73-70	Isoch Rcv Channel Mask High Set	0000 0000h
77-74	Isoch Rcv Channel Mask High Clr	0000 0000h
7B-78	Isoch Rcv Channel Mask Low Set	0000 0000h
7F-7C	Isoch Rcv Channel Mask Low Clr	0000 0000h
83-80	Interrupt Event Set	0000 0000h
87-84	Interrupt Event Clear	0000 0000h
8B-88	Interrupt Mask Set	0000 0000h
8F-8C	Interrupt Mask Clear	0000 0000h
93-90	Isoch Xmit Interrupt Event Set	0000 0000h
97-94	Isoch Xmit Interrupt Event Clear	0000 0000h
9B-98	Isoch Xmit Interrupt Mask Set	0000 0000h
9F-9C	Isoch Xmit Interrupt Mask Clear	0000 0000h
A3-A0	Isoch Rcv Interrupt Event Set	0000 0000h
A7-A4	Isoch Rcv Interrupt Event Clear	0000 0000h
AB-A8	Isoch Rcv Interrupt Mask Set	0000 0000h
AF-AC	Isoch Rcv Interrupt Mask Clear	0000 0000h
B3-B0	Initial Bandwidth Available	0000 0000h
B7-B4	Initial Channels Available Hi	FFFFFFFFh
BB-B8	Initial Channels Available Lo	FFFFFFFFh
DB-BC	RESERVED	-

DF-DC	Fairness Control	0000 0000h
E3-E0	Link Control Set	0000 0000h
E7-E4	Link Control Clear	0000 0000h
EB-E8	Node ID	0000 0000h
EF-EC	PHY Control	0000 0000h
F3-F0	Isochronous Cycle Timer	0000 0000h
F4-FF	RESERVED	-
103-100	Async Request Filter High Set	0000 0000h
107-104	Async Request Filter High Clear	0000 0000h
10B-108	Async Request Filter Low Set	0000 0000h
10F_10C	Async Request Filter Low Clear	0000 0000h
113-110	Physical Request Filter High Set	0000 0000h
117-114	Physical Request Filter High Clear	0000 0000h
11B-118	Physical Request Filter Low Set	0000 0000h
11F-11C	Physical Request Filter Low Clear	0000 0000h
120-123	Physical Upper Bound	0000 0000h
124-17F	RESERVED	-
183-180	Async Request Xmit Context Set	0000 0000h
187-184	Async Request Xmit Context Clr	0000 0000h
18F-18C	Async Request Xmit Command Ptr	0000 0000h
1A3-1A0	Async Response Xmit Context Set	0000 0000h
1A7-1A4	Async Response Xmit Context Clr	0000 0000h
1AF-1AC	Async Response Xmit Cmd Ptr	0000 0000h
1C3-1C0	Async Request Rcv Context Set	0000 0000h
1C7-1C4	Async Request Rcv Context Clr	0000 0000h
1CF-1CC	Async Request Rcv Command Ptr	0000 0000h
1E3-1E0	Async Response Rcv Context Set	0000 0000h
1E7-1E4	Async Response Rcv Context Clr	0000 0000h
1EF-1EC	Async Response Rcv Command Ptr	0000 0000h
203-200	Isoch Xmit Context 0 Set	0000 0000h
207-204	Isoch Xmit Context 0 Clr	0000 0000h
20F-20C	Isoch Xmit Context 0 Cmd Ptr	0000 0000h
213-210	Isoch Xmit Context 1 Set	0000 0000h
217-214	Isoch Xmit Context 1 Clr	0000 0000h
21F-21C	Isoch Xmit Context 1 Cmd Ptr	0000 0000h
223-220	Isoch Xmit Context 2 Set	0000 0000h
227-224	Isoch Xmit Context 2 Clr	0000 0000h
22F-22C	Isoch Xmit Context 2 Cmd Ptr	0000 0000h
233-230	Isoch Xmit Context 3 Set	0000 0000h
237-234	Isoch Xmit Context 3 Clr	0000 0000h
23F-23C	Isoch Xmit Context 3 Cmd Ptr	0000 0000h
243-240	Isoch Xmit Context 4 Set	0000 0000h
247-244	Isoch Xmit Context 4 Clr	0000 0000h
24F-24C	Isoch Xmit Context 4 Cmd Ptr	0000 0000h
253-250	Isoch Xmit Context 5 Set	0000 0000h
257-254	Isoch Xmit Context 5 Clr	0000 0000h
25F-25C	Isoch Xmit Context 5 Cmd Ptr	0000 0000h
263-260	Isoch Transmit Context 6 Set	0000 0000h
267-264	Isoch Transmit Context 6 Clr	0000 0000h

26F-26C	Isoch Transmit Context 6 Cmd Ptr	0000 0000h
273-270	Isoch Transmit Context 7 Set	0000 0000h
277-274	Isoch Transmit Context 7 Clr	0000 0000h
27F-27C	Isoch Transmit Context 7 Cmd Ptr	0000 0000h
3FF-280	RESERVED	-
403-400	Isoch Receive Context 0 Set	0000 0000h
407-404	Isoch Receive Context 0 Clr	0000 0000h
40F-40C	Isoch Receive Context 0 Command Ptr	0000 0000h
410	Isoch Receive Context 0 Match	0000 0000h
420	Isoch Receive Context 1 Set	0000 0000h
424	Isoch Receive Context 1 Clr	0000 0000h
42C	Isoch Receive Context 1 Command Ptr	0000 0000h
430	Isoch Receive Context 1 Match	0000 0000h
440	Isoch Receive Context 2 Set	0000 0000h
444	Isoch Receive Context 2 Clr	0000 0000h
44C	Isoch Receive Context 2 Command Ptr	0000 0000h
450	Isoch Receive Context 2 Match	0000 0000h
460	Isoch Receive Context 3 Set	0000 0000h
464	Isoch Receive Context 3 Clr	0000 0000h
46C	Isoch Receive Context 3 Command Ptr	0000 0000h
470	Isoch Receive Context 3 Match	0000 0000h
7FF-480	RESERVED	-

1394 PHY Registers

Table 5 – 1394 PHY Register Map

Offset	7	6	5	4	3	2	1	0
0000b	PS	R	Physical ID					
0001b	Gap Count						IBR	RHB
0010b	Total Ports				-	Extended		
0011b	Delay				-	Max Speed		
0100b	Power Class			Jitter			Cont	LC
0101b	Multi	Accel	PE	Tout	PF	Loop	ISBR	WT
0110b	RESERVED							
0111b	Port Select				-	Page Select		
1000b	Register 0 (Page Select)							
1001b	Register 1 (Page Select)							
1010b	Register 2 (Page Select)							
1011b	Register 3 (Page Select)							
1100b	Register 4 (Page Select)							
1101b	Register 5 (Page Select)							
1110b	Register 6 (Page Select)							
1111b	Register 7 (Page Select)							

Abbreviation

RO: Read Only.
WO: Write Only. (register value can not be read by the software)
RW: Read / Write.
RW1C: Read / Write of "1" clears bit to zero.

In register descriptions, the column "Default" indicates the power-on default value of register bit(s), while "Attribute" indicates the access type of register bit(s).

7 Register Descriptions

1394 Host Controller Configuration Registers

The 1394 host controller interface follows the Open HCI (OHCI) interface specification. The configuration registers are located in the function 0 PCI configuration space.

Header Registers

Offset 1-0h: Vendor ID Default: 1106h

Bit	Attribute	Default	Description
15-0	RO	1106h	VIA Technologies ID Code

Offset 3-2h: Device ID Default: 3403h

Bit	Attribute	Default	Description
15-0	RO	3403h	Device ID Code

Offset 5-4h: PCI Command Default: 0000h

Bit	Attribute	Default	Description
15-11	RO	0	Reserved
10	RW	0	Interrupt Disable 0: Enable 1: Disable
9	RW	0	Fast Back-to-Back Cycle Enable
8	RW	0	SERR# Enable
7	RW	0	Wait Cycle Control
6	RW	0	Parity Checking 0: Ignore parity errors. 1: Perform parity check and take normal action on detected parity errors.
5	RW	0	VGA Palette Snooping
4	RW	0	Memory Write and Invalidate
3	RW	0	Respond To Special Cycle
2	RW	0	PCI Master Function 0: Disable 1: Enable
1	RW	0	Memory Space Access 0: Disable 1: Enable Access to 1394 Memory
0	RW	0	I/O Space Access Does not respond to I/O space.

Offset 7-6h: PCI Status Default: 0210h

Bit	Attribute	Default	Description
15	RO	0	Detected Parity Error
14	RO	0	Signaled System Error (SERR#)
13	RW1C	0	Received Master Abort 0: No master abort generated. 1: Master abort generated by 1394 controller. Set by the 1394 interface logic if it generates a master abort while acting as a master. This bit may be cleared by software by writing a one to this bit position.
12	RW1C	0	Received Target Abort 0: No Target Abort Received. 1: Target Abort Received by 1394 Controller. Set by the 1394 interface logic if it receives a target abort while acting as a master. This bit may be cleared by software by writing a one to this bit position.
11	RO	0	Signaled Target Abort
10-9	RO	01b	DEVSEL# Timing 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	Data Parity Error Detected
7	RO	0	Fast Back-to-Back Capable
6	RO	0	User Definable Features
5	RO	0	66 MHz Capable
4	RO	1b	Capability List
3	RO	0	Interrupt Status Bit
2-0	RO	0	Reserved

Offset 8h: Revision Code Default: nnh

Bit	Attribute	Default	Description
7-0	RO	nnh	Revision Code

Offset 0B-9h: Class Code Default: 0C0010h

Bit	Attribute	Default	Description
23-0	RO	0C0010h	Class Code

Offset 0Ch: Cache Line Size Default: 00h

Bit	Attribute	Default	Description
7-0	RW	0	Cache Line Size

Offset 0Dh: Latency Timer Default: 00h

Bit	Attribute	Default	Description
7-3	RW	0	Latency Timer Count PCI burst cycles generated by the VT6315N can last indefinitely as long as PCI GNT# remains active. If GNT# is negated after the burst is initiated, the VT6315N limits the duration of the burst to the number of PCI Bus clocks specified in this field.
2-0	RO	0	Reserved

Offset 0Eh: Header Type Default: 80h

Bit	Attribute	Default	Description
7-0	RO	80h	Header Type

Offset 0Fh: Built In Self Test Default: 00h

Bit	Attribute	Default	Description
7	RO	0	BIST Support
6-0	RO	0	Reserved

Offset 13-10h: OHCI CSR Memory Mapped IO (MMIO) Base Default: 0000 0000h

Bit	Attribute	Default	Description
31-11	RW	0	Base Address (2048-Byte Space)
10-4	RO	0	Reserved
3	RO	0	Prefetchable Reads 0 to indicate that the register space is not prefetchable.
2-1	RO	0	Type Reads 0 to indicate that the address range is in the 16-bit I/O address space.
0	RO	0	Resource Type Reads 0 to indicate a request for memory space.

Offset 17-14h: CSR IO Base Address Default: 0000 0001h

Bit	Attribute	Default	Description
31-7	RW	0	Base Address (128-Byte Space)
6-4	RO	0	Reserved
3	RO	0	Prefetchable Reads 0 to indicate that the register space is not prefetchable.
2-1	RO	0	Type Reads 0 to indicate that the address range is in the 16-bit I/O address space.
0	RO	1b	Resource Type Reads 1 to indicate a request for I/O space.

Offset 2D-2Ch: Subsystem Vendor ID Default: 1106h

Bit	Attribute	Default	Description
15-0	RO	1106h	Subsystem Vendor ID From EEPROM

Offset 2F-2Eh: Subsystem ID Default: 3403h

Bit	Attribute	Default	Description
15-0	RO	3403h	Subsystem ID From EEPROM

Offset 33-30h: Reserved

Offset 34h: Capability Pointer Default: 50h

Bit	Attribute	Default	Description
7-0	RO	50h	Capability Pointer An offset address from the start of the configuration space.

Offset 3B-35h: Reserved

Offset 3Ch: Interrupt Line Default: 00h

Bit	Attribute	Default	Description
7-0	RW	0	Interrupt Line This field is used to communicate with software the interrupt line that the interrupt pin is connected to.

Offset 3Dh: Interrupt Pin Default: 01h

Bit	Attribute	Default	Description
7-0	RO	01h	Interrupt Pin 01h = Drives INTA#

Offset 3Eh: Minimum Grant Default: 00h

Bit	Attribute	Default	Description
7-0	RO	0	Minimum Grant

Offset 3Fh: Maximum Latency Default: 20h

Bit	Attribute	Default	Description
7-0	RO	20h	Maximum Latency

Offset 4F-40h: Reserved

Power Management Registers (Offset 7F-50h)

Offset 50h: Capability ID Default: 01h

Bit	Attribute	Default	Description
7-0	RO	01h	Capability ID

Offset 51h: Next Pointer Default: 00h

Bit	Attribute	Default	Description
7-0	RO	0	Next Pointer Reads 0 to indicate that there are no additional items in the Capabilities List.

Offset 53-52h: Power Management Capabilities Default: E403h

Bit	Attribute	Default	Description
15	RO	1b	PME# Can Be Asserted From D3cold 0: Not capable 1: Capable
14	RO	1b	PME# Can Be Asserted From D3hot 0: Not capable 1: Capable
13	RO	1b	PME# Can Be Asserted From D2 0: Not capable 1: Capable
12	RO	0	PME# Can Be Asserted From D1 0: Not capable 1: Capable
11	RO	0	PME# Can Be Asserted From D0 0: Not supported 1: Supported
10	RO	1b	D2 Power Management State Supported 0: Not supported 1: Supported
9	RO	0	D1 Power Management State Supported 0: Not supported 1: Supported
8-6	RO	000b	3.3V Auxiliary Current Required 000: None (device is self powered) 001: 55 mA 010: 100 mA 011: 160 mA 100: 220 mA 101: 270 mA 110: 320 mA 111: 375 mA
5	RO	0	Device-Specific Initialization Required 0: Not required 1: Required
4	RO	0	Reserved
3	RO	0	PME Clock 0: No PCI clock is required. 1: PCI clock is required for PME# generation.
2-0	RO	011b	Specification Version Reads 011b to indicate that this function complies with Revision 1.2 of the PCI Power Management Interface Specification.

Offset 55-54h: Power Management Control / Status Default: 0000h

Bit	Attribute	Default	Description
15	RW1C	0	PME Status This bit is set when the function would normally assert the PME# signal independent of the state of the PME_Enable bit. Writing a "1" will clear this bit and cause the function to stop asserting PME# (if enabled).
14-13	RO	0	Data Scale Scaling factor to use when interpreting the value of the Data register.
12-9	RW	0	Data Select Used to select which data is to be reported through the Data register and Data Scale field.
8	RW	0	PME Enable 0: PME# assertion disabled. 1: PME# assertion enabled.
7-2	RO	0	Reserved
1-0	RW	00b	Power State These bits indicate the current power state and are used to change to a new power state. If an attempt is made to write a code corresponding to an unsupported state, the write of these bits is ignored and no state change occurs. 00: D0 01: D1 10: D2 11: D3hot

Offset 7F-56h: Reserved

MSI Capability Structure (Offset 97–80h)

Offset 83-80h: MSI Control Register Structure Default: 0180 0005h

Bit	Attribute	Default	Description
31-25	RO	0	Reserved
24	RW	1b	Per Vector Mask (PVM) Capable
23	RO	1b	64-bit Address Capable
22-20	RW	0	Multiple Message Enable
19-17	RO	0	Multiple Message Capable
16	RW	0	MSI Enable
15-8	RO	0	Next Pointer
7-0	RO	05h	Capability ID

Offset 87–84h: MSI Low Address Default: 0000 0000h

Bit	Attribute	Default	Description
31-2	RW	0	System-Specified Message Lower Address
1-0	RO	0	Reserved

Offset 8B–88h: MSI High Address Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	System-Specified Message Upper Address

Offset 8F–8Ch: MSI Data Register Default: 0000 0000h

Bit	Attribute	Default	Description
31-16	RO	0	Reserved
15-0	RW	0	System-Specified Message

Offset 93–90h: MSI Mask Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	The function is prohibited from generating the associated message for each mask bit that is set.

Offset 97–94h: MSI Pending Default: 0000 0000h

Bit	Attribute	Default	Description
31-1	RO	0	Reserved
0	RO	0	PVM Pending Bit 0

PCI Express Capability Structure (Offset AB–98h)

Offset 9B–98h: PCI Express Capability Default: 0011 C010h

Bit	Attribute	Default	Description
31-30	RO	0	Reserved
29-25	RO	0	Interrupt Message Number
24	RO	0	Slot Implemented
23-20	RO	1h EEPROM	Device/Port Type
19-16	RO	1h	Capability Version
15-8	RO	C0h	Next Pointer
7-0	RO	10h	Capability ID

Offset 9F–9Ch: PCI Express – Device Capability Default:0000 80C0h

Bit	Attribute	Default	Description
31-28	RO	0	Reserved
27-26	RO	0	Captured Slot Power Limit Scale
25-18	RO	0	Captured Slot Power Limit Value
17-16	RO	0	Reserved
15	RO	1b	RBEREN
14	RO	0	Power Indicator Present
13	RO	0	Attention Indicator Present
12	RO	0	Attention Button Present
11-9	RO	0	Endpoint L1 Acceptable Latency
8-6	RO	011b	Endpoint L0s Acceptable Latency
5	RO	0	Extended Tag Field Supported
4-3	RO	0	Phantom Functions Supported
2-0	RO	0	Maximum Payload Size Supported

Offset A1–A0h: PCI Express – Device Control Default: 0000h

Bit	Attribute	Default	Description
15	RO	0	Reserved
14-12	RW	0	Maximum Read Request Size
11	RO	0	Enable No Snoop
10	RW	0	AUX Power PM Enable
9	RO	0	Phantom Functions Enable
8	RO	0	Extended Tag Field Enable
7-5	RW	0	Maximum Payload Size
4	RO	0	Enable Relaxed Ordering
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

Offset A3–A2h: PCI Express – Device Status Default: 0010h

Bit	Attribute	Default	Description
15-6	RO	0	Reserved
5	RO	0	Transaction Pending
4	RO	1b	AUX Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected
1	RW1C	0	Non-Fatal Error Detected
0	RW1C	0	Correctable Error Detected

Offset A7–A4h: PCI Express – Link Capability Default: 0004 CC11h

Bit	Attribute	Default	Description
31-24	RO	0	Port Number
23-21	RO	0	Reserved
20	RO	0	DLACT_RPT_CAP
19	RO	0	SPRS_DOWN
18	RO	1b	CLK_PM_CAP
17-15	RO	001b	L1 Exit Latency
14-12	RO	100b	L0s Exit Latency
11-10	RO	11b	ASPM Support
9-4	RO	01h	Maximum Link Width
3-0	RO	1h	Maximum Link Speed

Offset A9–A8h: PCI Express – Link Control Default: 0000h

Bit	Attribute	Default	Description
15-9	RO	0	Reserved
8	RW	0	CFG_CLKREQEN
7	RW	0	Extended Synch
6	RW	0	Common Clock Configuration
5-4	RO	0	Reserved
3	RW	0	Read Completion Boundary (RCB)
2	RO	0	Reserved
1-0	RW	0	ASPM Control

Offset AB–AAh: PCI Express – Link Status Default: 1011h

Bit	Attribute	Default	Description
15-14	RO	0	Reserved
13	RO	0	DL_LNKACT
12	RO	1b	Slot Clock Configuration
11-10	RO	0	Reserved
9-4	RO	01h	Negotiated Link Width
3-0	RO	1h	Link Speed

PCI Express Extended Space (Offset 13B–100h)

Offset 103–100h: PCI Express – Advanced Error Reporting Enhanced Capability Default: 1301 0001h

Bit	Attribute	Default	Description
31-20	RO	130	Next Capability
19-16	RO	1h	Capability Version
15-0	RO	0001h	PCI Express Extended Capability ID

Offset 107–104h: PCI Express – Uncorrectable Error Status Default: 0000 0000h

Bit	Attribute	Default	Description
31-21	RO	0	Reserved
20	RW1C	0	Unsupported Request Error Status
19	RW1C	0	ECRC Error Status (Optional)
18	RW1C	0	Malformed TLP Status
17	RW1C	0	Receiver Overflow Status (Optional)
16	RW1C	0	Unexpected Completion Status
15	RW1C	0	Completer Abort Status (Optional)
14	RW1C	0	Completion Timeout Status
13	RW1C	0	Flow Control Protocol Error Status (Optional)
12	RW1C	0	Poisoned TLP Status
11-6	RO	0	Reserved
5	RO	0	Surprise Down Error Status
4	RW1C	0	Data Link Protocol Error Status
3-1	RO	0	Reserved
0	RW	0	Undefined

Offset 10B–108h: PCI Express – Uncorrectable Error Mask Default: 0000 0030h

Bit	Attribute	Default	Description
31-21	RO	0	Reserved
20	RW	0	Unsupported Request Error Mask
19	RW	0	ECRC Error Mask (Optional)
18	RW	0	Malformed TLP Mask
17	RW	0	Receiver Overflow Mask (Optional)
16	RW	0	Unexpected Completion Mask
15	RW	0	Completer Abort Mask (Optional)
14	RW	0	Completion Timeout Mask
13	RW	0	Flow Control Protocol Error Mask (Optional)
12	RW	0	Poisoned TLP Mask
11-6	RO	0	Reserved
5	RW	1b	Surprise Down Error Mask
4	RW	1b	Data Link Protocol Error Mask
3-1	RO	0	Reserved
0	RW	0	Undefined

Offset 10F–10Ch: PCI Express – Uncorrectable Error Severity Default: 0006 2031h

Bit	Attribute	Default	Description
31-21	RO	0	Reserved
20	RW	0	Unsupported Request Error Severity
19	RW	0	ECRC Error Severity (Optional)
18	RW	1b	Malformed TLP Severity
17	RW	1b	Receiver Overflow Error Severity (Optional)
16	RW	0	Unexpected Completion Error Severity
15	RW	0	Completer Abort Error Severity (Optional)
14	RW	0	Completion Timeout Error Severity
13	RW	1b	Flow Control Protocol Error Severity (Optional)
12	RW	0	Poisoned TLP Severity
11-6	RO	0	Reserved
5	RW	1b	Surprise Down Error Severity
4	RW	1b	Data Link Protocol Error Severity
3-1	RO	0	Reserved
0	RW	1b	Undefined

Offset 113–110h: PCI Express – Correctable Error Status Default: 0000 0000h

Bit	Attribute	Default	Description
31-14	RO	0	Reserved
13	RW1C	0	Advisory Non-Fatal Error Status
12	RW1C	0	Replay Timer Timeout Status
11-9	RO	0	Reserved
8	RW1C	0	REPLAY_NUM Rollover Status
7	RW1C	0	Bad DLLP Status
6	RW1C	0	Bad TLP Status
5-1	RO	0	Reserved
0	RW1C	0	Receiver Error Status (Optional)

Offset 117–114h: PCI Express – Correctable Error Mask Default: 0000 2000h

Bit	Attribute	Default	Description
31-14	RO	0	Reserved
13	RW	1b	Advisory Non-Fatal Error Mask
12	RW	0	Replay Timer Timeout Mask
11-9	RO	0	Reserved
8	RW	0	REPLAY_NUM Rollover Mask
7	RW	0	Bad DLLP Mask
6	RW	0	Bad TLP Mask
5-1	RO	0	Reserved
0	RW	0	Receiver Error Mask (Optional)

Offset 11B–118h: PCI Express – Advanced Error Capability and Control Default: 0000 00A0h

Bit	Attribute	Default	Description
31-9	RO	0	Reserved
8	RW	0	ECRC Check Enable
7	RO	1b	ECRC Check Capable
6	RW	0	ECRC Generation Enable
5	RO	1b	ECRC Generation Capable
4-0	RO	0	First Error Pointer

Offset 12B–11Ch: PCI Express – Header Log Registers Default: 0h

Bit	Attribute	Default	Description
127-0	RO	0	Header of TLP associated with error

Offset 133–130h: Device Serial Number Enhanced Capability Default: 0001 0003h

Bit	Attribute	Default	Description
31-20	RO	0	Device Serial Number Next Pointer (DSNNXPTR)
19-16	RO	01h	Device Serial Number Capability Version (DSNCAP_VER)
15-0	RO	0003h	Extended Capability ID

Offset 137–134h: Device Serial Number [31:0] – Lower Default: 0000 0000h

Bit	Attribute	Default	Description
31-16	RO	0	DSNR1_LO
15-0	RO	0	DSNR0_LO

Offset 13B–138h: Device Serial Number [63:32] – Upper Default: 0000 1106h

Bit	Attribute	Default	Description
31-16	RO	0	DSNR1_UP
15-0	RO	1106h	DSNR0_UP

1394 OHCI-Link Memory Space Register
These registers occupy a 2048-byte space in system memory (offsets 0-7FFh). This address space begins at the address contained in the 1394 Configuration Space "Base Address Register" (Function 0 Configuration Space Offset 10h).

All registers must be accessed as 32-bit words on 32-bit boundaries. Writes to reserved addresses have undefined results and reads from reserved addresses return indeterminate data. Unless specified otherwise, all register fields default to 0 and are unchanged after a 1394 bus reset.

Some registers are designated as Set and Clear registers. These registers are in pairs, where a read of either address will return the current contents of the register. Data written to the Set register address is assumed to be a bit mask where one bits determine which bits should be set. Data written to the Clear register address is assumed to be a bit mask where one bits determine which bits should be cleared.

Offset 3-0h: Version Default: —h

Bit	Attribute	Default	Description
31-0	RO	—	Version OHCI 1.0 Mode: 0001 0000b OHCI 1.1 Mode: 0001 0010b

Offset 4-7h: Reserved

Offset 0B-8h: Asynchronous Transmit Retries Default: 0000 0000h

Bit	Attribute	Default	Description
31-29	RO	0	Second Limit Count in Seconds (modulo 8). These bits and the Cycle Limit bits below define a time limit for retry attempts when the outbound dual-phase retry protocol is in use.
28-16	RO	0	Cycle Limit Count in Cycles (modulo 8000). These bits and the Second Limit bits above define a time limit for retry attempts when the outbound dual-phase retry protocol is in use.
15-12	RO	0	Reserved
11-8	RW	0	Max Physical Response Retries Specifies how many times to attempt to retry the transmit operation for the physical response packet when a "busy" or "ack_type_error" acknowledge is received from the target node. This value is used only for responses to physical requests.
7-4	RW	0	Max AT Response Retries Specifies to the Asynchronous Transmit Response subsystem how many times to attempt to retry the transmit operation for the response packet when a "busy" or "ack_type_error" acknowledge is received from the target node. This value is used only for responses sent by software via the Asynchronous Transmit Response DMA context.
3-0	RW	0	Max AT Request Retries Specifies to the Asynchronous Transmit DMA Request subsystem how many times to attempt to retry the transmit operation for a packet when a "busy" or "ack_type_error" acknowledge is received from the target node. This value is used only for responses sent by software via the Asynchronous Transmit Request DMA context.

Autonomous CSR Resources

The VT6315N implements the 1394 "Compare-and-Swap" bus management registers, the Configuration ROM Header, and the "Bus Info Block". It also allows access to the first 1K bytes of the configuration ROM.

Atomic compare-and-swap transactions, when accessed from the 1394 bus, are autonomous without software intervention. To access these bus management resource registers via the PCI bus, the software first loads the CSR Data register with a new data value to be loaded, then it loads the CSR Compare register with the expected value. Finally, it writes the CSR Control register with the selected value of the resource. This initiates a compare-and-swap operation. When complete, the CSR Control register "done" bit will be set and the CSR Data register will contain the value of the selected resource prior to the host-initiated compare-and-swap operation.

Bus Management CSR Registers

1394 requires certain 1394 bus management resource registers to be accessible only via 32-bit read and 32-bit lock (compare-and-swap) transactions. These special bus management resource registers are implemented on-chip:

CSR Address	CSR Select	Register Name	Hardware or Bus Reset
FFFF F000 021C	00	Bus Manager ID	0000 003F
FFFF F000 0220	01	Bandwidth Available	0000 1333
FFFF F000 0224	10	Channels Available Hi	FFFF FFFF
FFFF F000 0228	18	Channels Available Lo	FFFF FFFF

Offset 0F-0Ch: CSR Data Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	CSR Data Data to be stored if comparison is successful.

Offset 13-10h: CSR Compare Data Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	CSR Compare Data Data to be compared with existing value of CSR resource.

Offset 17-14h: CSR Control Default: 8000 0000h

Bit	Attribute	Default	Description
31	RW	1b	CSR Done Set when a compare-swap operation is completed. Reset whenever this register is written.
30-2	RO	0	Reserved
1-0	RW	00b	CSR Resource Select 00: Bus Manager ID 01: Bandwidth Available 10: Channels Available High 11: Channels Available Low

Offset 1B-18h: Configuration ROM Header Default: 0000 0000h

Bit	Attribute	Default	Description
31-24	RW	0	Bus Info Block Length Length of the Bus Information Block in doublewords.
23-16	RW	0	CRC Length Length of the block protected by the CRC (a value of 4 indicates that the CRC only protects the configuration ROM header).
15-0	RW	0	ROM CRC Value Default value loaded from GUID ROM if present (default is undefined if GUID ROM is not present). Must be set prior to setting the "HC Control" register "Link Enable" bit.

Offset 1F-1Ch: 1394 Bus ID Default: 3133 3934h

Bit	Attribute	Default	Description
31-0	RO	3133 3934h	Bus ID This register maps to the 1st 32-bit word of the bus info block. Always reads 3133 3934h (ASCII "1394").

Offset 23-20h: 1394 Bus Options Default: F000 0002h

This register maps to the 2nd quadword of the bus info block.

Bit	Attribute	Default	Description
31	RW	1b	Isochronous Resource Manager Capable 0: Not capable 1: Capable
30	RW	1b	Cycle Master Capable 0: Not capable 1: Capable
29	RW	1b	Isochronous Capable 0: Not capable 1: Capable
28	RW	1b	Bus Manager Capable 0: Not capable 1: Capable
27	RW	0	Power Management Capable 0: Not capable 1: Capable
26-24	RO	0	Reserved
23-16	RW	0	Cycle Clock Acc 1394 Bus Management Field. This field must be written with valid data prior to setting the "HC Control" register "link enable" bit.
15-12	RW	0	Received Block Write Request Packet Max Length 1394 Bus Management Field. This field must be written with valid data prior to setting the "HC Control" register "link enable" bit. Received block write request packets with a length greater than the value contained in this field may generate an "ack_type_error".
11-8	RO	0	Reserved
7-6	RW	0	Configuration ROM Changed Since Last Bus Reset 0: Configuration ROM not changed. 1: Configuration ROM changed.
5-3	RO	0	Reserved
2-0	RW	010b	Max Link Speed

Offset 27-24h: Global Unique ID High Default: 0000 0000h

This register maps to the 3rd 32-bit word of the bus info block. Contents are cleared by hardware reset but are not affected by software reset. Read/Write if Rx44[0] is cleared, Read/Only if Rx44[0] is set.

Bit	Attribute	Default	Description
31-8	RW	0	Node Vendor ID 1394 Bus Management Field. Must be set prior to setting the "HC Control" register "link enable" bit.
7-0	RW	0	Chip ID High 1394 Bus Management Field. Must be set prior to setting the "HC Control" register "link enable" bit.

Offset 2B-28h: Global Unique ID Low Default: 0000 0000h

This register maps to the 4th 32-bit word of the bus info block. Contents are cleared by hardware reset but are not affected by software reset. Read/Write if Rx44[0] is cleared, Read/Only if Rx44[0] is set.

Bit	Attribute	Default	Description
31-0	RW	0	Chip ID Low 1394 Bus Management Field. Must be set prior to setting the "HC Control" register "link enable" bit.

Offset 33-2Ch: Reserved

Offset 37-34h: Configuration ROM Map Default: 0000 0000h

This register contains the start address within the memory space that maps to the start address of the 1394 configuration ROM. Only 32-bit word reads to the first 1K bytes of the configuration ROM will map to memory space.(all other transactions to this space will be rejected with an "ack_type_error"). The system address of the configuration ROM must start on a 1K-byte boundary. The first five 32-bit words of the configuration ROM space are mapped to the configuration ROM header and Bus Info Block, so the first five registers addressed by this register are not used. This register must be set to a valid address prior to setting the "HC Control" register "link enable" bit.

Bit	Attribute	Default	Description
31-10	RW	0	Configuration ROM Address Read requests to 1394 offsets FFFF F000 0400 through FFFF F000 03FC have the low-order 10 bits of the offset added to this register to determine the host memory address of the returned data value
9-0	RO	0	Reserved

Offset 3B-38h: Posted Write Address Low Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RO	0	Offset Low If the "Posted Write Error" bit is set in the Interrupt Events register, this and the "Posted Write Address High" register contain the 48 bits of the 1394 destination offset of the write request that resulted in the PCI error.

Offset 3F-3Ch: Posted Write Address High Default: 0000 0000h

Bit	Attribute	Default	Description
31-16	RO	0	Source ID The Bus Number and Node Number of the node which has issued the failed write request.
15-0	RO	0	Offset High If the "Posted Write Error" bit is set in the Interrupt Events register, this and the "Posted Write Address Low" register contain the 48 bits of the 1394 destination offset of the write request that resulted in the PCI error.

Offset 43-40h: Vendor ID Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RO	0	Vendor ID

Offset 44-4Fh: Reserved

HC Control Registers

The following two registers are a "set / clear" register pair. Writing to the "Set" register address sets selected bits in the control register where the written bit value is 1. Writing to the "Clear" register address clears selected bits in the control register where the written bit value is 1. Reading from either address returns the contents of the control register.

Offset 53-50h (Set), 57-54h (Clear): HC Control Default: 0000 0000h

Bit	Attribute	Default	Description
31-20	RO	0	Reserved
19	RO	0	Link Power Status 0: Prohibit Link to PHY Communications. 1: Permit Link to PHY Communications (link can use LREQs to perform PHY reads and writes). This bit has no effect on "Link On" status for the node (see Link Enable status below). Both software and hardware resets clear this bit.
18	RW	0	Posted Write Enable 0: All writes return "ack_pending". 1: Enable 2-deep posted write queue. Software should only change this bit when "Link Enable" is 0.
17	RW	0	Link Enable 0: Disable packets from being transmitted, received, or processed. 1: Enable packets to be transmitted, received, and processed Both software and hardware resets clear this bit. Software should not set this bit until the Configuration ROM mapping register is valid.
16	RW	0	Soft Reset When set, all on-chip 1394 states are reset, all FIFOs are flushed, and all registers are set to their hardware reset (default) values unless otherwise specified. PCI configuration registers are not affected. Hardware clears this bit automatically when the reset is complete (it reads 1 while the reset is in progress).
15-0	RO	0	Reserved

Offset 5F-58h: Reserved

Self-ID Control Registers

Offset 63-60h: Reserved

Offset 67-64h: Self ID Buffer Pointer Default: 0000 0000h

Bit	Attribute	Default	Description
31-11	RW	0	Self-ID Buffer Pointer Contains the base address of a 2K-byte buffer in host memory where received Self-ID packets are stored.
10-0	RO	0	Reserved

Offset 6B-68h: Self ID Count Default: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Self-ID Error 0: Self-ID packet received with no errors (this bit is automatically cleared after error-free reception of a Self-ID packet). 1: Error detected during most recent Self-ID packet reception (the contents of the Self-ID Buffer are undefined in this case).
30-24	RO	0	Reserved
23-16	RO	0	Self-ID Generation The value in this field is incremented automatically each time the Self-ID reception process begins. The value rolls over after reaching 255.
15-13	RO	0	Reserved
12-2	RO	0	Self-ID Size Contains the length in 32-bit words of Self-ID data that has been received. This field is cleared by 1394 bus reset.
1-0	RO	0	Reserved

Offset 6F-6Ch: Reserved

Channel Mask Registers

Offset 73-70h (Set), 77-74h (Clear): Iso Rcv Channel Mask High Default: 0000 0000h

Bit	Attribute	Default	Description
19	RW	0	Iso Channel Mask N+32 Bits 31-0 correspond to channel numbers 63-32. Writing 1 bits to offset 70 enables corresponding channels for receiving isochronous data. Writing 1 bits to offset 74 disables corresponding channels from receiving isochronous data.

Offset 7B-78h (Set), 7F-7Ch (Clear): Iso Rcv Channel Mask Low Default: 0000 0000h

Bit	Attribute	Default	Description
19	RW	0	Iso Channel Mask N+32 Bits 31-0 correspond to channel numbers 31-0. Writing 1 bits to offset 78 enables corresponding channels for receiving isochronous data. Writing 1 bits to offset 7C disables corresponding channels from receiving isochronous data.

Interrupt Registers

Offset 83-80h (Set), 87-84h (Clear): Interrupt Events Default: 0000 0000h

Bit	Attribute	Default	Description
31-27	RO	0	Reserved
26	RW	0	PHY Register Data Received PHY register data byte received (data byte not sent when register 0 received).
25	RW	0	Cycle Too Long More than 115 usec (but not more than 120 usec) elapsed between the start of sending a cycle start packet and the end of a subaction gap.
24	RW	0	Unrecoverable Error Error encountered that has forced the chip to stop operations of any or all subunits (e.g., when a DMA context sets its "ContextControl.Dead" bit).
23	RW	0	Cycle Inconsistent Cycle start received with a cycle count different from the value in the "Cycle Timer" register.
22	RW	0	Cycle Lost Expected cycle start not received (cycle start not received immediately after the first subaction gap after the "Cycle Sync" event or arbitration reset gap detected after a "Cycle Sync" event without an intervening cycle start).
21	RW	0	Cycle 64 Seconds Interrupt Bit 7 of the "Cycle Seconds Counter" has changed.
20	RW	0	Cycle Synch Interrupt New isochronous cycle started (least significant bit of the cycle count toggled).
19	RW	0	PHY Requested Interrupt The PHY has requested an interrupt using a status transfer.
18	RO	0	Reserved
17	RW	0	Bus Reset Entered The Phy has entered bus reset mode.
16	RW	0	Self-ID Complete Self-ID packet stream received.
15-10	RO	0	Reserved
9	RW	0	Lock Response Error Lock response sent to a serial bus register in response to a lock request but no "ack_complete" received.
8	RW	0	Posted Write Error A host bus error occurred while the chip was trying to write a 1394 write request (which had already been given an "ack_complete") into system memory.
7	RW	0	Isochronous ReceiveDMA Complete One or more Isochronous receive contexts have generated an interrupt (one or more bits have been set in the "Isochronous Receive Interrupt Event" register masked by the "Isochronous Receive Interrupt Mask" register).
6	RW	0	Isochronous Transmit DMA Complete One or more Isochronous transmit contexts have generated an interrupt (one or more bits have been set in the "Isochronous Transmit Interrupt Event" register masked by the "Isochronous Transmit Interrupt Mask" register).
5	RW	0	Response Packet Sent A packet was sent to an asynchronous receive response context buffer.

4	RW	0	Receive Packet Sent A packet was sent to an asynchronous receive request context buffer.
3	RW	0	Async Receive Response DMA Complete Conditionally set upon completion of an ARDMA Response context command descriptor.
2	RW	0	Async Receive Request DMA Complete Conditionally set upon completion of an ARDMA Request context command descriptor.
1	RW	0	Async Response Transmit DMA Complete Conditionally set upon completion of an ATDMA Response command.
0	RW	0	Async Request Transmit DMA Complete Conditionally set upon completion of an ATDMA Request command.

Offset 8B-88h (Set), 8F-8Ch (Clear): Interrupt Mask Default: 0000 0000h

The bits in this register (except for the Master Interrupt Enable bit in bit-31) correspond to the bits in the Interrupt Event register above. Zeros in these bits prevent the corresponding interrupt condition from generating an interrupt. Bits are set in the mask register by writing one bits to the "Set" address and cleared by writing one bits to the "Clear" address. The current value of the mask bits may be read from either address.

Bit	Attribute	Default	Description
31	RW	0	Master Interrupt Enable 0: Disable All Interrupt Events. 1: Generate interrupts per mask bits 0-26.
30-27	RO	0	Reserved
26-0	RW	0	Interrupt Mask (See Interrupt Event register.)

Offset 93-90h (Set), 97-94h (Clear): Iso Transmit Interrupt Events Default: 0000 0000h

Bit	Attribute	Default	Description
31-8	RO	0	Reserved
7-0	RW	0	Isochronous Transmit Context An interrupt is generated by an isochronous transmit context if an "Output Last DMA" command completes and its "i" bits are set to "interrupt always". Software clears the bits in this register by writing one bit to the "Clear" address. Bits in this register will only get set to one if the corresponding bits in the mask register are set to one.

Offset 9B-98h (Set), 9F-9Ch (Clear): Iso Transmit Interrupt Mask Default: 0000 0000h

Bit	Attribute	Default	Description
31-8	RO	0	Reserved
7-0	RW	0	Iso Transmit Context Mask Setting bits in this register enables interrupts to be generated by the corresponding isochronous transmit context.

Offset A3-A0h (Set), A7-A4h (Clear): Iso Receive Interrupt Events Default: 0000 0000h

Bit	Attribute	Default	Description
31-4	RO	0	Reserved
3-0	RW	0	Isochronous Receive Context An interrupt is generated by an isochronous receive context if an "Input Last DMA" command completes and its "i" bits are set to "interrupt always". Software clears the bits in this register by writing one bit to the "Clear" address. Bits in this register will only get set to one if the corresponding bits in the mask register are set to one.

Offset AB-A8h (Set), AF-ACh (Clear): Iso Receive Interrupt Mask Default: 0000 0000h

Bit	Attribute	Default	Description
31-4	RO	0	Reserved
3-0	RW	0	Iso Receive Context Mask Setting bits in this register enables interrupts to be generated by the corresponding isochronous receive context.

Offset B3-B0h: Initial Bandwidth Available Default: 0000 0000h

Bit	Attribute	Default	Description
31-13	RO	0	Reserved
12-0	RW	0	Initial Bandwidth Available

Offset B7-B4h: Initial Channels Available High Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	Initial Channels Available

Offset BB-B8h: Initial Channels Available Low Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	Initial Channels Available

Offset DB-BCh: Reserved

Link Control Registers

Offset DF-DCh: Fairness Control Default: 0000 0000h

Bit	Attribute	Default	Description
31-8	RO	0	Reserved
7-0	RO	0	Requests Per Fairness Interval The number of request packets allowed to be transmitted per fairness interval.

Offset E3-E0h (Set), E7-E4h (Clear): Link Control Default: 0000 0000h

This register contains the control flags that enable and configure the link core protocol portions of the chip. It contains controls for the receiver and cycle timer.

Bit	Attribute	Default	Description
31-22	RO	0	Reserved
21	RW	0	Cycle Master 0: Received cycle start packets will be accepted to maintain synchronization with the node that is sending them. 1: If the PHY has sent notification that it is root, a cycle start packet will be generated every time the cycle timer rolls over, based on the setting of the "Cycle Source" bit. This bit is cleared automatically if the "Cycle Too Long" interrupt event occurs and cannot be set until the "Cycle Too Long" interrupt event bit is cleared.
20	RW	0	Cycle Timer Enable 0: Cycle timer offset will not count. 1: Cycle Timer offset will count cycles of the 24.576 MHz clock and roll over at the appropriate time based on the settings of the above bits.
19-11	RO	0	Reserved
10	RW	0	Receive PHY Packet 0: All PHY packets received outside of the self-ID phase are ignored. 1: The receiver will accept incoming PHY packets into the AR request context if the AR request context is enabled. This bit does not control receipt of self-ID packets.
9	RW	0	Receive Self-ID 0: All self-ID packets are ignored. 1: The receiver will accept incoming self-identification packets. Before setting this bit, software must ensure that the self-ID buffer pointer register contains a valid address.
8-0	RO	0	Reserved

Offset EB-E8h: Node ID Default: 0000 0000h

This register contains the CSR address for the node on which this chip resides. The 16-bit combination of the Bus Number and Node Number fields is referred to as the "Node ID". The Node Number field is updated when register 0 is sent from the PHY. This can happen either because software requested a read from the PHY through the PHY Control register or because the PHY is sending the register (most likely due to a bus reset).

Bit	Attribute	Default	Description
31	RW	0	ID Valid 0: No valid node number (cleared by bus reset). 1: Valid node number received from PHY.
30	RW	0	Root This bit is set to 0 or 1 during bus reset. 0: Attached PHY is not root. 1: Attached PHY is root.
29-28	RO	0	Reserved
27	RO	0	Cable Power Status 0: PHY reports cable power status is not OK. 1: PHY reports cable power status is OK.
26-16	RO	0	Reserved
15-6	RW	0	Bus Number Used to identify the specific 1394 bus to which this node belongs when multiple 1394-compatible buses are connected via a bridge (set to 3FFh by bus reset).
5-0	RW	0	Node Number The physical node number established by the PHY during self-identification and automatically set to the value received from the PHY after the self-identification phase. If the PHY sets this field to 63 (all ones), all link-level transmits are disabled.

1394 PHY Control Registers

Offset EF-ECh: PHY Control Default: 0000 0000h

This register is used to read or write a PHY register. To read or write, the address of the register is written into the Register Address field. For reads the "Read Register" bit is set (when the request has been sent to the PHY, the "Read Register" bit is cleared automatically by the chip). When transmitting the request, the first clock for LREQ for the register read/write portion will be bit-11 of this register followed by bit-10, etc, finishing with bit-8 for register reads and bit-0 for register writes. When the PHY returns the register through a status transfer, the "Read Done" bit is set. The address of the register received is placed in the "Read Address" field and the contents in the "Read Data" field. The first bits of data received on the status transfer for the register are placed in bits 27 (D[0]) and 26 (D[1]) of this register. For writes, the value to write is written to the "Write Data" field and the "Write Register" bit is set. The "Write Register" bit is cleared automatically by the chip when the write request has been sent to the PHY.

Bit	Attribute	Default	Description
31	RW	0	Read Done Indicates that a read request has been completed and valid information is contained in the Read Data and Read Address fields. Cleared when the "Read Register" bit is set. It is set by the chip when a register transfer is received from the PHY.
30-28	RO	0	Reserved
27-24	RW	0	Read Address The address of the register most recently received from the PHY.
23-16	RW	0	Read Data The contents of the register most recently received from the PHY
15	RW	0	Read Register Used to initiate a read request from a PHY register (must not be set at the same time as the "Write Register" bit). Cleared by the chip when the request has been sent.
14	RW	0	Write Register Used to initiate a write request to a PHY register (must not be set at the same time as the "Read Register" bit). Cleared by the chip when the request has been sent.
13-12	RO	0	Reserved
11-8	RW	0	Register Address The address of the PHY register to be read or written.
7-0	RW	0	Write Data The data to be written to the PHY (ignored for reads).

Cycle Timer Registers

Offset F3-F0h: Isochronous Cycle Timer Default: 0000 0000h

This register shows the current cycle number and offset. When the chip is cycle master, this register is transmitted with the cycle start message. When it is not cycle master, this register is loaded with the data field in an incoming cycle start. In the event that the cycle start message is not received, the fields continue incrementing on their own (when the "Cycle Timer Enable" field is set in the "Link Control" register) to maintain a local time reference.

Bit	Attribute	Default	Description
31-25	RW	0	Cycle Seconds This field counts seconds ("Cycle Count" rollovers) modulo 128.
24-12	RW	0	Cycle Count This field counts cycles ("Cycle Offset" rollovers) modulo 8000.
11-0	RW	0	Cycle Offset This field counts 24.576 MHz clocks modulo 3072 (125 usec).

Offset FF-F4h: Reserved

Filter Registers

Offset 100h (Set), 104h (Clear): Async Req Filter High Default: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Async Request Resources All Buses 0: Asynchronous requests received from non-local bus nodes will be accepted only if the bit which is set corresponds to the node number (see the remaining bits of this register and the "Async Request Filter Low" register). 1: All asynchronous requests received from non-local bus nodes will be accepted. Bus reset does not affect the value of this bit.
30-0	RW	0	Async Request Resource "N" If set to one for local bus node number N+32, asynchronous requests received from that node number will be accepted. The bit number corresponds to the node number + 32. Bus reset sets all bits of this field to 0.

Offset 108h (Set), 10Ch (Clear): Async Request Filter Low Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	Async Request Resource "N" If set to one for local bus node number N, asynchronous requests received from that node number will be accepted. The bit number corresponds to the node number. Bus reset sets all bits of this field to 0.

Offset 110h (Set), 114h (Clear): Physical Request Filter High Default: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Physical Request Resources All Buses 0: Asynchronous physical requests received from non-local bus nodes will be accepted only if the bit which is set corresponds to the node number (see the remaining bits of this register and the "Physical Request Filter Low" register). 1: All asynchronous physical requests received from non-local bus nodes will be accepted. Bus reset does not affect the value of this bit.
30-0	RW	0	Physical Request Resource "N" If set to one for local bus node number N+32, asynchronous physical requests received from that node number will be accepted. The bit number corresponds to the node number + 32. Bus reset sets all bits of this field to 0.

Offset 118h (Set), 11Ch (Clear): Physical Request Filter Low Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	Physical Request Resource "N" If set to one for local bus node number N, asynchronous physical requests received from that node number will be accepted. The bit number corresponds to the node number. Bus reset sets all bits of this field to 0.

Offset 123-120h: Physical Upper Bound Default: 0000 0000h

Bit	Attribute	Default	Description
31-0	RW	0	Physical Upper Bound

Asynchronous Transmit & Receive Context Registers

Offset 180h (Set), 184h (Clear): Async Request Transmit Context Default: 0000 0000h

Offset 1A0h (Set), 1A4h (Clear): Async Response Transmit Context Default: 0000 0000h

Offset 1C0h (Set), 1C4h (Clear): Async Request Receive Context Default: 0000 0000h

Offset 1E0h (Set), 1E4h (Clear): Async Response Receive Context Default: 0000 0000h

These registers are the Context Control registers for Asynchronous Transmit Requests and Responses and Asynchronous Receive Requests and Responses, respectively. They contain bits for control of options, operational state, and status for a DMA context. The bit layout for both registers is given below:

Bit	Attribute	Default	Description
31-16	RO	0	Reserved
15	RW	0	Run This bit is set and cleared by software to enable descriptor processing for a context. The chip will clear this bit automatically on a hardware or software reset. Before software sets this bit, the active bit must be clear and the Command Pointer register for the context must contain a valid descriptor block address and a Z value that is appropriate for the descriptor block address. Software may stop the chip from further processing of a context by clearing this bit. When cleared, the chip will stop processing of the context in a manner that will not impact the operation of any other context or DMA controller. This may require a significant amount of time. If software clears a run bit for an isochronous context while the chip is processing a packet for the context, it will continue to receive or transmit the packet and update the descriptor status.

			It will then stop at the conclusion of that packet. If the run bit is cleared for a non-isochronous context, the chip will stop processing at a convenient point and put the descriptors in a consistent state (e.g., status updated if a packet was sent and acknowledged). Clearing the bit may have other side effects that are DMA controller dependent. This is described in the sections that cover each of the DMA controllers.
14-13	RO	0	Reserved
12	RW	0	Wake When software adds to a list of descriptors for a context, the chip may have already read the descriptor that was at the end of the list before it was updated. This bit provides a semaphore to indicate that the list may have changed. If the chip had fetched a descriptor and the indicated branch address had a Z value of zero, it will reread the pointer value when the wake bit is set. If, on the reread, the Z value is still zero, then the end of the list has been reached and the chip will clear the active bit. If, however, the Z value is now non-zero, the chip will continue processing. If the wake bit is set while the chip is active and has a Z value of non-zero, it takes no special action. The chip will clear this bit before it reads or rereads a descriptor. The wake bit should not be set while the run bit is zero.
11	RW	0	Dead This bit is set by the chip to indicate a fatal error in processing a descriptor. When set, the active bit is cleared. This bit is cleared when software clears the run bit or on a hardware or software reset.
10	RW	0	Active This bit is set by the chip when software sets the run bit or sets the wake bit while the run bit is set. The chip will clear this bit when 1. a branch has been indicated by a descriptor, but the Z value of the branch address is 0; 2. the software has cleared the run bit, and the chip has reached a safe stopping point; 3. the dead bit has been set; 4. a hardware or software reset has occurred; or 5. a bus reset has occurred for asynchronous transmit contexts (request and response). When this bit is 0 and the run bit is 0, the chip will set the Interrupt Event bit for the context.
9-8	RO	0	Reserved
7-5	RW	000	Speed (Async Receive Contexts Only) This field indicates the speed at which the packet was received or transmitted: 000: 100 Mbits/sec 001: 200 Mbits/sec 010: 400 Mbits/sec 011: -reserved- 1xx: Reserved
4-0	RW	0	Ack / Err Code Following an "Output Last" command, the received "Ack Code" or "Event Error Code" is indicated in this field. Possible values are: "Ack Complete", "Ack Pending", Ack Busy X", "Ack Data Error", "Ack Type Error", "Event Tcode Error", "Event Missing Ack", "Event Underrun", "Event Descriptor Read", "Event Data Read", "Event Timeout", "Event Flushed", and "Event Unknown" (see "Table 6" on the following page for descriptions and values for these codes).

Offset 18Ch: Async Request Transmit Context Command Pointer Default: 0000 0000h

Offset 1Ach: Async Response Transmit Context Command Pointer Default: 0000 0000h

Offset 1CCh: Async Request Receive Context Command Pointer Default: 0000 0000h

Offset 1ECh: Async Response Receive Context Command Pointer Default: 0000 0000h

Table 6 – Packet Event Codes

Code	Name	DMA	Meaning
00/10	Event Tcode Error	AT, AR, IT, IR, IT	A bad Tcode is associated with this packet. The packet was flushed.
01/11	Event Short Packet		The received data length was less than the packet's data length (IR packet-per-buffer mode only).
02/12	Event Long Packet	IR	The received data length was greater than the packet's data length (IR packet-per-buffer mode only).
03/13	Event Missing Ack	AT	A subaction gap was detected before an ack arrived
04/14	Event Underrun	AT, IT	An underrun occurred on the corresponding FIFO and the packet was truncated.
05/15	Event Overrun	IR	A receive FIFO overflowed during the reception of an isochronous packet.
06/16	Event Descriptor Read	AT, AR, IT, IR	An unrecoverable error occurred while the Host Controller was reading a descriptor block.
07/17	Event Data Read	AT, IT	An error occurred while the Host Controller was attempting to read from host memory in the data stage of descriptor processing.
08/18	Event Data Write	AR, IR, IT	An error occurred while the Host Controller was attempting to write to host memory in the data stage of descriptor processing.
09/19	Event Bus Reset	AR	Identifies a PHY packet in the receive buffer as being the synthesized bus reset packet
0A/1A	Event Timeout	AT	Indicates that the asynchronous transmit response packet expired and was not transmitted
0B	Event Tcode Error	AT	A bad Tcode is associated with this packet. The packet was flushed.
0C-0D/ 1B-1D	Reserved		
0E/1E	Event Unknown	AT, AR, IT, IR	An error condition has occurred that cannot be represented by any other defined event codes
0F/1F	Event Flushed	AT	Sent by the link side of the output FIFO when asynchronous packets are being flushed due to a bus reset
11	Ack Complete	AT, AR, IT, IR	The destination node has successfully accepted the packet. If the packet was a request subaction, the destination node has successfully completed the transaction and no response subaction shall follow. The ack / err code for transmitted PHY, isochronous and broadcast packets, none of which yield an ack code, will be set by hardware to "Ack Complete" unless an "Event Underrun" or "Event Data Read" occurs.
12	Ack Pending	AT, AR	The destination node has successfully accepted the packet. If the packet was a request subaction, a response subaction will follow at a later time. This code is not returned for a response subaction.
13	Reserved		
14	Ack Busy X	AT	The packet could not be accepted after max "ATretries" attempts and the last Ack received was "Ack Busy X."
15	Ack Busy A	AT	The packet could not be accepted after max "ATretries" attempts and the last Ack received was "Ack Busy A." OHCI does not support the dual phase retry protocol for transmitted packets, so this Ack should not be received.
16	Ack Busy B	AT	The packet could not be accepted after max "ATretries" attempts and the last Ack received was "Ack Busy B" (see note for "Ack Busy A").
17-1C	Reserved		
1D	Ack Data Error	AT, IR	The destination node could not accept the block packet because the data field failed the CRC check or because the length of the data block payload did not match the length contained in the "Data Length" field. This code is not returned for any packet that does not have a data block payload.
1E	Ack Type Error	AT, AR	Returned when a received block write request or received block read request is greater than "max_rec"
1F	Reserved		

Asynchronous Transmit Context Registers

Offset 200h (Set), 204h (Clear): Isoch Transmit Context 0 Default: 0000 0000h

Offset 210h (Set), 214h (Clear): Isoch Transmit Context 1 Default: 0000 0000h

Offset 220h (Set), 224h (Clear): Isoch Transmit Context 2 Default: 0000 0000h

Offset 230h (Set), 234h (Clear): Isoch Transmit Context 3 Default: 0000 0000h

Offset 240h (Set), 244h (Clear): Isoch Transmit Context 4 Default: 0000 0000h

Offset 250h (Set), 254h (Clear): Isoch Transmit Context 5 Default: 0000 0000h

Offset 260h (Set), 264h (Clear): Isoch Transmit Context 6 Default: 0000 0000h

Offset 270h (Set), 274h (Clear): Isoch Transmit Context 7 Default: 0000 0000h

These registers are the Context Control registers for isochronous Transmit Contexts 0-7. Each context consists of two registers: a Command Pointer and a Context Control register. The Command Pointer is used by software to tell the controller where the context program begins. The Context Control register controls the context's behavior and indicates current status. The bit layout for the Context Control registers is given below:

Bit	Attribute	Default	Description
31-30	RO	0	Reserved
29	RW	0	Cycle Match Enable In general, when set to one the context will begin running only when the 13-bit "Cycle Match" field matches the 13-bit "Cycle Count" in the Cycle Start packet. The effects of this bit however are impacted by the values of other bits in this register. Once the context becomes active, this bit is cleared automatically by the chip.
28-16	RW	0	Cycle Match Contains a 13-bit value corresponding to the 13-bit "Cycle Count" field. If the "Cycle Match Enable" bit is set, this ITDMA context will become enabled for transmits when the bus cycle time "Cycle Count" value equals the value in this field.
15	RW	0	Run This bit is set and cleared by software to enable descriptor processing for a context. The chip will clear this bit automatically on a hardware or software reset. Before software sets this bit, the active bit must be clear and the Command Pointer register for the context must contain a valid descriptor block address and a Z value that is appropriate for the descriptor block address. Software may stop the chip from further processing of a context by clearing this bit. When cleared, the chip will stop processing of the context in a manner that will not impact the operation of any other context or DMA controller. This may require a significant amount of time. If software clears a run bit while the chip is processing a packet for the context, it will continue to receive or transmit the packet and update the descriptor status. It will then stop at the conclusion of that packet. Clearing the bit may have other side effects that are DMA controller dependent. This is described in the sections that cover each of the DMA controllers.
14-13	RO	0	Reserved
12	RW	0	Wake When software adds to a list of descriptors for a context, the chip may have already read the descriptor that was at the end of the list before it was updated. This bit provides a semaphore to indicate that the list may have changed. If the chip had fetched a descriptor and the indicated branch address had a Z value of zero, it will reread the pointer value when the wake bit is set. If, on the reread, the Z value is still zero, then the end of the list has been reached and the chip will clear the active bit. If, however, the Z value is now non-zero, the chip will continue

			processing. If the wake bit is set while the chip is active and has a Z value of non-zero, it takes no special action. The chip will clear this bit before it reads or rereads a descriptor. The wake bit should not be set while the run bit is zero.
11	RW	0	Dead This bit is set by the chip to indicate a fatal error in processing a descriptor. When set, the active bit is cleared. This bit is cleared when software clears the run bit or on a hardware or software reset.
10	RW	0	Active This bit is set by the chip when software sets the run bit or sets the wake bit while the run bit is set. The chip will clear this bit when 1. a branch has been indicated by a descriptor, but the Z value of the branch address is 0; 2. the software has cleared the run bit, and the chip has reached a safe stopping point; 3. the dead bit has been set; or 4. a hardware or software reset has occurred. When this bit is cleared and the run bit is clear, the chip will set the Interrupt Event bit for the context.
9-5	RO	0	Reserved
4-0	RW	0	Ack / Err Code Following an "Output Last" command, the received "Ack Code" or "Event Error Code" is indicated in this field. Possible values are: "Ack Complete", "Ack Pending", Ack Busy X", "Ack Data Error", "Ack Type Error", "Event Tcode Error", "Event Missing Ack", "Event Underrun", "Event Descriptor Read", "Event Data Read", "Event Timeout", "Event Flushed", and "Event Unknown" (see "Table 6" on the previous page for descriptions and values for these codes).

Offset Address 20Ch: Isoch Transmit Context 0 Command Pointer Default: 0000 0000h

Offset Address 21Ch: Isoch Transmit Context 1 Command Pointer Default: 0000 0000h

Offset Address 22Ch: Isoch Transmit Context 2 Command Pointer Default: 0000 0000h

Offset Address 23Ch: Isoch Transmit Context 3 Command Pointer Default: 0000 0000h

Offset Address 24Ch: Isoch Transmit Context 4 Command Pointer Default: 0000 0000h

Offset Address 25Ch: Isoch Transmit Context 5 Command Pointer Default: 0000 0000h

Offset Address 26Ch: Isoch Transmit Context 6 Command Pointer Default: 0000 0000h

Offset Address 27Ch: Isoch Transmit Context 7 Command Pointer Default: 0000 0000h

Asynchronous Receive Context Registers

Offset 400h (Set), 404h (Clear): Isoch Receive Context 0 Default: 0000 0000h

Offset 420h (Set), 424h (Clear): Isoch Receive Context 1 Default: 0000 0000h

Offset 440h (Set), 444h (Clear): Isoch Receive Context 2 Default: 0000 0000h

Offset 460h (Set), 464h (Clear): Isoch Transmit Context 3 Default: 0000 0000h

These registers are the Context Control registers for isochronous Receive Contexts 0-3. Each context consists of three registers: a Command Pointer, a Context Control register, and a Context Match register. The Command Pointer is used by software to tell the controller where the context program begins. The Context Control register controls the context's behavior and indicates current status. The Context Match Register is used to start transmitting from a context program on a specified cycle number. The bit layout for the Context Control registers is given below:

Bit	Attribute	Default	Description
31	RW	0	Buffer Fill 0: Each received packet is placed in a single buffe.r 1: Received packets are placed back-to-back to completely fill each receive buffer. If the "Multi-Channel Mode" bit is set, this bit must also be set. This bit must not be changed while the "Active" bit is set.
30	RW	0	Isoch Header 0: The packet header is stripped from received isochronous packets. 1: Received packets will include the isochronous packet header (the header will be stored first in memory followed by the payload). The end of the packet will be marked with a "Transfer Status" (bits 15-0 of this register) in the first word followed by a 16-bit time stamp indicating the time of the most recently received "Cycle Start" packet.
29	RW	0	Cycle Match Enable 0: Context will begin running immediately. 1: Context will begin running only when the 13-bit "Cycle Match" field in the "Context Match" register matches the 13-bit "Cycle Count" in the Cycle Start packet. The effects of this bit are impacted by the values of other bits in this register. Once the context becomes active, this bit is cleared automatically by the chip.
28	RW	0	Multi-Channel Mode 0: The context will receive packets for a single channel. 1: The context will receive packets for all isochronous channels enabled in the "IR Channel Mask High" and "IR Channel Mask Low" registers (the channel number in the "Context Match" register is ignored). If more than one Context Control register has the Multi-Channel Mode bit set, unspecified behavior will result.
27-16	RO	0	Reserved
15	RW	0	Run This bit is set and cleared by software to enable descriptor processing for a context. The chip will clear this bit automatically on a hardware or software reset. Before software sets this bit, the active bit must be clear and the Command Pointer register for the context must contain a valid descriptor block address and a Z value that is appropriate for the descriptor block address. Software may stop the chip from further processing of a context by clearing this bit. When cleared, the chip will stop processing of the context in a manner that will not impact the operation of any other context or DMA controller. This may require a significant amount of time. If software clears the run bit while the chip is processing a packet for the context, it will continue to receive or transmit the packet and update descriptor status. It will then stop at the conclusion of that packet. Clearing the bit may have other side effects that are DMA controller dependent. This is described in the sections that cover each of the DMA controllers.
14-13	RO	0	Reserved
12	RW	0	Wake When software adds to a list of descriptors for a context, the chip may have already read the descriptor that was at the end of the list before it was updated. This bit provides a semaphore to indicate that the list may have changed. If the chip had fetched a descriptor and the indicated branch address had a Z value of zero, it will reread the pointer value when the wake bit is set. If, on the reread, the Z value is still zero, then the end of the list has been reached and the chip will clear the active bit. If, however, the Z value is now non-zero, the chip will continue processing. If the wake bit is set while the chip is active and has a Z value of non-zero, it takes no special action. The chip will clear this bit before it reads or rereads a descriptor. The wake bit should not be set while the run bit is zero.

11	RW	0	Dead This bit is set by the chip to indicate a fatal error in processing a descriptor. When set, the active bit is cleared. This bit is cleared when software clears the run bit or on a hardware or software reset.
10	RW	0	Active This bit is set by the chip when software sets the run bit or sets the wake bit while the run bit is set. The chip will clear this bit when 1) a branch has been indicated by a descriptor, but the Z value of the branch address is 0; 2) the software has cleared the run bit, and the chip has reached a safe stopping point; 3) the dead bit has been set; or 4) a hardware or software reset has occurred. When this bit is cleared and the run bit is clear, the chip will set the Interrupt Event bit for the context.
9-7	RO	0	Reserved
6-5	RW	0	Speed This field indicates the speed at which the packet was received or transmitted: 00: 100 Mbits/sec 01: 200 Mbits/sec 10: 400 Mbits/sec 11: Reserved
4-0	RW	0	Ack / Err Code Following an "Input" command, this field contains the error code. For "Buffer Fill" mode, possible values are: "Ack Complete", "Ack Data Error", "Event Overrun", "Event Descriptor Read", "Event Data Write", and "Event Unknown" (see "Table 6" for descriptions and values for these codes). For "Packet-Per-Buffer" mode, possible values are: "Ack Complete", "Ack Data Error", "Event Short Packet", "Event Long Packet", "Event Overrun", "Event Descriptor Read", "Event Data Write", and "Event Unknown" (see "Table 6" for descriptions and values for these codes).

Offset 40Ch: Isoch Receive Context 0 Command Pointer Default: 0000 0000h

Offset 42Ch: Isoch Receive Context 1 Command Pointer Default: 0000 0000h

Offset 44Ch: Isoch Receive Context 2 Command Pointer Default: 0000 0000h

Offset 46Ch: Isoch Receive Context 3 Command Pointer Default: 0000 0000h

Offset 410h: Isoch Receive Context 0 Match Default: 0000 0000h

Offset 430h: Isoch Receive Context 1 Match Default: 0000 0000h

Offset 450h: Isoch Receive Context 2 Match Default: 0000 0000h

Offset 470h: Isoch Receive Context 3 Match Default: 0000 0000h

1394 PHY Register Map Descriptions

Field	Bits	Type	Def	Description
Physical_ID	6	RO	-	The address of this node determined during self-identification. A value of 63 indicates a malconfigured bus where the link must not transmit any packets.
R	1	RO	-	A setting of one indicates that this node is the root.
PS	1	RO	-	Cable Power status.
RHB	1	RW	0	Root hold-off bit. A setting of one instructs the chip to attempt to become the root during the next tree identification process.
IBR	1	RW	0	Initiate bus reset. A setting of one instructs the chip to initiate a bus reset immediately (without arbitration). This causes assertion of the reset state for 166 us and is self-clearing.
Gap Count	6	RW	3Fh	Used to configure the arbitration timer setting in order to optimize gap times according to the topology of the bus.
Extended	3	RO	111	Constant value of seven
Total Ports	5	RO	011	One ports
Max Speed	3	RO	010	Supports 98.304, 196.608, and 393.216 Mbit/s
Delay	4	RO	0	Worse case repeater delay = 144 ns
Link Control	1	RW	1	Link Control. Cleared or set by software to control the value of the L bit transmitted in the node's Self-ID packet 0.
Contender	1	RW	Pin CMC	Contender. Cleared or set by software to control the value of the C bit transmitted in the first self-ID packet.
Power Class	3	RW	Pins PC [0:2]	Power class. This information will be copied to bits 21-23 of the first self-ID packet.
Jitter	3	RO	0	Repeater delay; 20ns variation max
WT	1	RW	0	Watchdog enable. Controls whether loop, power fail, and timeout interrupts are indicated to the link when the link is in sleep. Also determines whether interrupts are indicated to the internal link when resume operations start.
ISBR	1	RW	0	Initiate short (arbitrated) bus reset. A write of one to this bit instructs the chip to arbitrate and issue a short bus reset. This bit is self-clearing.
Loop	1	RW	0	Loop detect. A write of one to this bit clears it to zero.
Power Fail	1	RW	1	Cable power failure detect. Set to one when the PS bit changes from one to zero. A write of one to this bit clears it to zero.
Timeout	1	RW	0	Arbitration state machine timeout. A write of one to this bit clears it to zero.
Port Event	1	RW	0	Port event detect. The chip sets this bit to one if any of connected, Bias, Disabled or Fault change for a port whose Int_enable bit is one. The chip also sets this bit to one if resume operations commence and Resume_int is one. A write of one to this bit clears it to zero.
Enable Acceleration	1	RW	0	Enable arbitration acceleration. When set to one, the chip must use the enhancements specification in IEEE P1394a 4.0.
Enable Multi	1	RW	0	Enable multi-speed packet concatenation.
Page Select	3	RW	000	Selects which of eight possible PHY register pages are accessible through the window at PHY register address 1000b through 1111b, inclusive.
Port Select	4	RW	0000	If the page selected by Page_select presents per port information, this field selects which port's registers are accessible through the window at PHY register addresses 1000b through 1111b, inclusive.

PHY Register Page 0 - Port Status

The Port Status page is used to access configuration and status information for the PHY's port. The port is selected by writing zero to Page_select and the desired port number to Port_select in the PHY register at address 0111.

Offset	7	6	5	4	3	2	1	0
1000b	Disa	Bias	Conn	Child	Bstat		Astat	
1001b	RESERVED			Fault	IntEn	Negotiated Speed		
1010b	RESERVED							
1011b	RESERVED							
1100b	RESERVED							
1101b	RESERVED							
1110b	RESERVED							
1111b	RESERVED							

Field	Bits	Type	Def	Description
Astat	2	RO	-	TPA line state for the port 00 = invalid 01 =1 10 =0 11 =z
Bstat	2	RO	-	Same encoding as Astat
Child	1	RO	-	1 indicates the port is a child, 0 a parent. The meaning of this bit is undefined from the time a bus reset is detected until the chip transitions to state T1:Child Handshake during the tree identify process (see 4.4.2.2 in IEEE 1394-1995)
Conncted	1	RO	0	One indicates the port is connected, zero indicates it is disconnected. The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed.
Bias	1	RO	-	One indicates that bias voltage is detected (possible connection). The value reported by this bit is filtered by hysteresis logic to reduce multiple status changes caused by contact scrape when a connector is inserted or removed.
Disabled	1	RW	0	When set to one, the port is disabled. The value of this bit subsequent to a power reset is implementation-dependent, but should be a strappable option.
Negotiated Speed	3	RO	-	Indicates the maximum speed negotiated between this port and its immediately connected port. 000 – 98.304 Mbit/s 001 - and 196.608 Mbit/s 010 - and 393.216 Mbit/s
Interrupt Enable	1	RW	0	Enable port event interrupts. When set to one, the chip sets Port_event to one if any of Connected, Bias, Disabled or Fault (for this port) change state.
Fault	1	RW	0	Set to one if an error is detected during a suspend or resume operation. A write of one to this bit clears it to zero.

PHY Register Page 1 - Vendor Identification

The Vendor Identification page is used to identify the VT6315N's vendor and compliance level. The page is selected by writing one to Page_select in the PHY register at address 0111.

Offset	7	6	5	4	3	2	1	0
1000b	Compliance Level							
1001b	RESERVED							
1010b	Vendor ID							
1011b								
1100b								
1101b	Product ID							
1110b								
1111b								

Field	Bits	Type	Default	Description
Compliance Level	8	RO	1	"1" indicates IEEE P1394a
Vendor ID	24	RO	00 40 63	The company ID or Organizationally Unique Identifier (OUI) of the manufacturer of the PHY. The most significant byte of Vendor_ID appears at PHY register location 1010 and the least significant at 1100.
Product ID	24	RO	30 60 00	The meaning of this number is determined by the company or organization that has been granted Vendor_ID. The most significant byte of Product_ID appears at PHY register location 1101 and the least significant at 1111.

PHY Register Page 7 - Vendor-Dependent

The vendor-dependent page provides registers set aside for use by the PHY's vendor. The page is selected by writing seven to Page_select in the PHY register at address 0111.

Offset	7	6	5	4	3	2	1	0
1000b	Reserved for Test (Do Not Access)							
1001b	Reserved for Test (Do Not Access)							
1010b	Reserved for Test (Do Not Access)							
1011b	Reserved for Test (Do Not Access)							
1100b	Reserved for Test (Do Not Access)							
1101b	Reserved for Test (Do Not Access)							
1110b	Reserved for Test (Do Not Access)							
1111b	Reserved for Test (Do Not Access)							

8 Functional Descriptions

8.1 PHY General Description

Cable Interface
The VT6315N provides a 2-port physical layer function in a cable IEEE 1394-1995 or 1394a-2000 network. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for half duplex packet reception and transmission.

Data bits to be transmitted through the cable ports are latched internally in the VT6315N in synchronization with the 49.152-MHz system clock. During transmission the encoded data is transmitted differentially on the TPB cable pair(s) and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded Strobe information is received on the TPB cable pair. The received data-strobe information is resynchronized to local PLL clocks and the retiming buffer can tolerate clock variation up to +/-100ppm with 4K bytes at 393.216 Mbps, 2K bytes at 196.608 Mbps, and 1K bytes at 98.304 Mbps.

Both the TPA and TPB cable interfaces (see figure below) incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by internal logic to determine the arbitration status. The TPA channel generates the cable common-mode voltage. The value of this common mode voltage is used during arbitration to detect the speed of the next packet transmission by the peer PHY. In addition, VT6315N adds a current source and a connection detect circuit at TPA channel. When TPBIAS is driven low, the connection detect circuit is used to detect the presence or absence of a peer PHY at the other end of a cable connection. The TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable suspend, resume and active status.

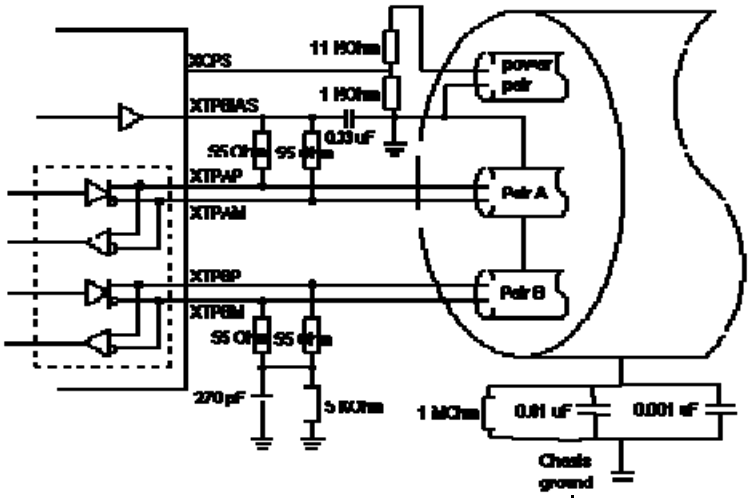


Figure 3 – Cable Interface

8.2 PHY Circuit Description

Pinless PLL and Clock Generation
The VT6315N PHY requires an external 24.576 MHz crystal as a reference. An external clock can also be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216 MHz reference clock. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded Strobe and Data information. A 49.152 MHz clock signal is used for resynchronization of the received data. The PLL requires no external filter components, referred to as "pinless PLL", saving board implementation cost.

Power Down and Auto Power Save
The power down function stops operation of the PLL and disables all circuits except the connection detection circuits and bias detection circuits at the XTPBIAS pins. Port transmitter and receiver circuitry are also disabled automatically when the port is disabled, suspended, or disconnected.

Data Transmission
Data bits to be transmitted through the cable ports are latched internally in synchronization with the 49.152 MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304/196.608/392.216 Mbps (referred to as S100, S200, and S400 speed, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

Data Reception
During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are collected into two-bit, four-bit or eight-bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152 MHz system clock and sent to the LLC. The retiming buffer can tolerate clock variation up to +/-100 ppm (compared to peer PHY) with 4K bytes at 393.216 Mbps, 2K bytes at 196.608 Mbps, and 1K bets at 98.304 Mbps. The received data is also transmitted (repeated) to the other active (connected) cable ports.

TPBIAS
Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage to determine the speed of the next packet transmission (speed signaling) during arbitration. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the peer PHY bias voltage. The VT6315N provides two independent 1.84V nominal bias voltages at the XTPBIAS pins. The bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. The bias voltage source must be stabilized by an external filter capacitor of 0.33 μF.

Bias-Detector / Connect-Detector / Bias-Discharger
The VT6315N supports suspend / resume / disable functions as defined in the IEEE P1394a V4.0 specification. The suspend mechanism allows pairs of directly connected ports to be placed into a low power state while maintaining a port-to-port connection between 1394 bus segments. While in a low power state, a port is unable to transmit or receive data transaction packets. However, a port in a low power state is capable of detecting connection status changes and detecting incoming TPBIAS. When all three ports are suspended, all circuits except the connect-detect circuits and bias-detect circuits are powered down, resulting in significant power savings. The connect-detect circuit monitors the value of incoming TPA pair common-mode voltage when local TPBIAS is inactive. A very small current source charges the XTPBIAS pin to almost VCC when the cable is not connected. Before the connect-detect circuit is enabled, the VT6315N enables a bias-discharger to improve the later-on connect-detect quality. Both the cable bias-detect monitor and connect-detect monitor are used in connect / suspend / resume / disable signaling. For additional details of suspend / resume / disable operation, refer to the IEEE P1394a V4.0 specification.

Twisted-Pair TPA and TPB
The line drivers operate in a high-impedance current mode, and are designed to work with external 110 Ohm line-termination resistor networks in order to match the 110 Ohm cable impedance. One network is provided at each end of all twisted-pair cable. Each network is composed of a pair of series-connected 55 Ohm resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair TPA pins is connected to its corresponding XTPBIAS pin. The midpoint of the pair of resistors that is directly connected to the twisted-pair B pins is coupled to ground through a parallel RC network with recommended values of 5K Ohm and 270 pF. The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits.

Bandgap Current Generation
An external resistor connected between the XRES pin and ground sets the driver output current, as well as internal operating currents. This current-setting resistor has a value of 5.6 kΩ ±1%.

Power Off
When the power supply of the VT6315N is removed while the twisted-pair cables are connected, the VT6315N transmitter / receiver circuitry and the XTPBIAS pin presents a high impedance state. As the consequence, peer PHYs see the VT6315N as unconnected.

9 Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	ºC	—
T_C	Case Operating Temperature	0	85	ºC	—
V_{CC}	Power Supply Voltage	-0.5	4.0	V	—
V_I	Input Voltage	-0.5	5.5	V	—
V_O	Output Voltage at any output	-0.5	VCC + 0.5	V	—
V_{ESD}	Electrostatic Discharge	—	2	kV	Human Body Model

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

DC Characteristics

Operating Conditions:
T_C = 0~+55ºC
V_{CCPCI} V_{CCSUS} V_{CCUSB} = 3.3V±5%
V_{CORE} = 1.2V±5%
GND = 0V

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.50	0.8	V	—
V_{IH}	Input High Voltage	2.0	VCC+0.5	V	—
V_{OL}	Output Low Voltage	—	0.45	V	I_{OL}=4.0 mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH}=-1.0 mA
I_{IL}	Input Leakage Current	—	±10	μA	0 < V_{IN} < VCC
I_{OZ}	Tristate Leakage Current	—	±20	μA	0.45 < V_{OUT} < VCC

PCI Express REFCLK DC Specifications and AC Timing Requirements

Symbol	Parameter	100 MHz Input		Unit
		Min	Max	
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns
V_{IH}	Differential Input High Voltage	+150		mV
V_{IL}	Differential Input Low Voltage		-150	mV
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV
$V_{CROSS\ DELTA}$	Variation of VCROSS over all rising clock edges		+140	mV
V_{RB}	Ring-back Voltage Margin	-100	+100	mV
T_{STABLE}	Time before V_{RB} is allowed	500		ps
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm
$T_{PERIOD\ ABS}$	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847	10.203	ns
$T_{CCJITTER}$	Cycle to Cycle jitter		150	ps
V_{MAX}	Absolute Max input voltage		+1.15	V
V_{MIN}	Absolute Min input voltage		- 0.3	V
Duty Cycle	Duty Cycle	40	60	%
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching		20	%
ZC-DC	Clock source DC impedance	40	60	Ω

Note: Refer Section 2.1.3. REFCLK AC Specifications of PCI Express Card Electromechanical Specification, Rev. 2.0 for more details.

Recommended Operating Conditions - PHY

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		3	3.3	3.6	V
V_{IL1}	Input Low Voltage	PHYCMC, PHYPC[0:2]	–0.5		1.1	V
V_{IH1}	Input High Voltage	PHYCMC, PHYPC[0:2]	2.2		V_{CC} + 0.5	V
V_{IL2}	Input Low Voltage	GRSTZ	–0.5		0.9	V
V_{IH2}	Input High Voltage	GRSTZ	2.1		V_{CC} + 0.5	V
I_O	TPBIAS Output Current		–1.2		1.2	mA
I_{OL} , I_{OH}	Output High/Low Current		–16		16	mA
T_{PU}	Power-up Reset Time	GRSTZ input	35			ms
V_{ID}	Differential Input Voltage	TPA/TPB cable input during data reception	118		260	mV
V_{IDA}	Differential Input Voltage	TPA/TPB cable input during arbitration	168		265	mV
V_{IC}	Common Mode Input Voltage		1.165		2.515	V
	Receive Input Jitter	S400			±0.5	ns
	Receive Input Skew	S400			±0.5	ns
F_{XSTAL}	Crystal or External Clock Frequency	XI	24.5735	24.576	24.5785	MHz

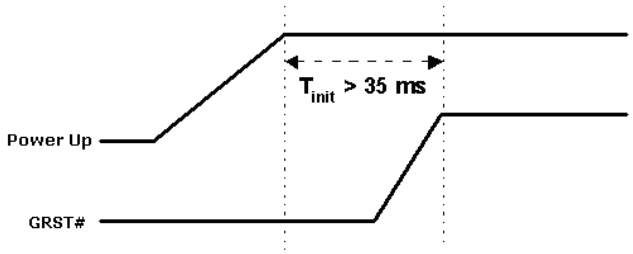


Figure 4 – Power-up Reset Timing

1394 Analog Signal Characteristics

TPA/TPB Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OD}	Output Signal Amplitude	Differential, 54.9 Ω	172	265	mV
		S400		0.2	ns
		S400		0.1	ns
	Data Output Rise/Fall Time	S100(10%-90%)	0.5	3.2	ns
		S200(10%-90%)	0.5	2.2	ns
		S400(10%-90%)	0.5	1.2	ns
V_{OFF}	OFF State Differential Voltage	Peak-to-peak, differential, 54.9 Ohm		20	mV
I_{OD}	Driver Difference Current	Speed signaling OFF, XTPAP, XTPAM, XTPBP, XTPBM	–1.05	1.05	mA
	Common Mode Speed Signaling Current	S100, XTPBP, XTPBM	–0.81	–0.44	mA
		S200, XTPBP, XTPBM	–4.84	–2.53	mA
		S400, XTPBP, XTPBM	–12.4	–8.10	mA

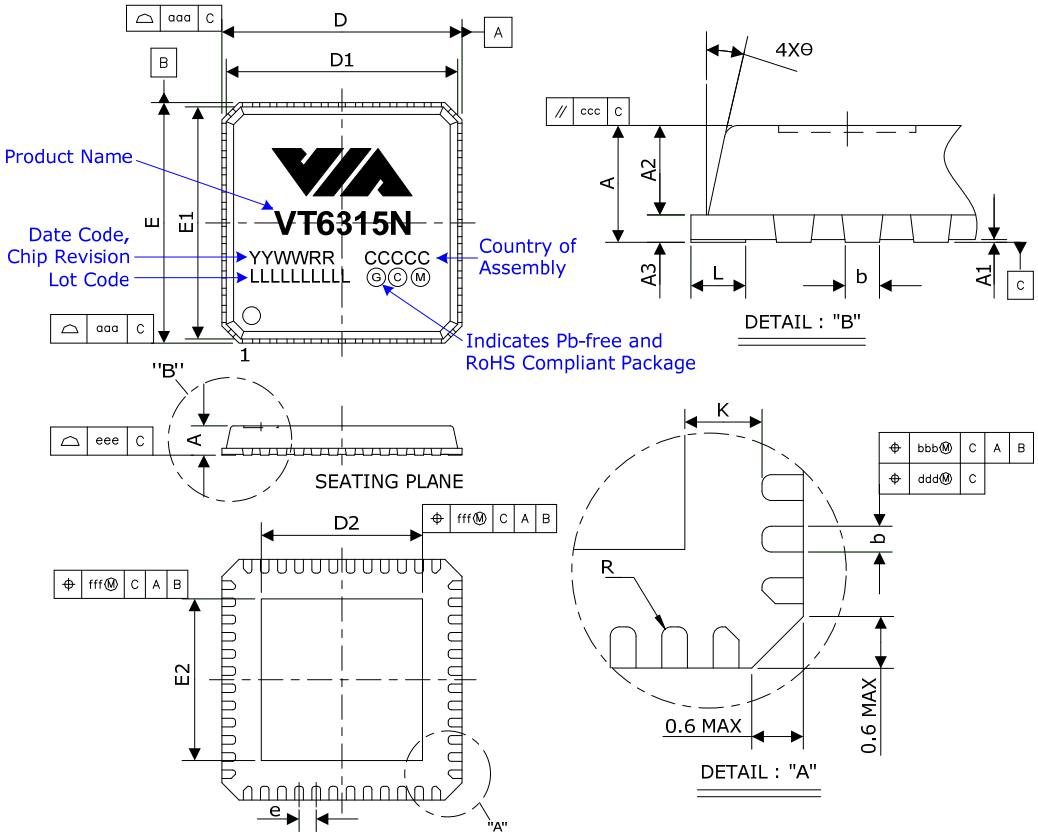
TPA/TPB Receiver Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Z_{ID}	Differential Input Impedance	Driver disabled			4	pF
				14		kΩ
Z_{IC}	Common Mode Impedance	Driver disabled			24	pF
			20			kΩ
V_{TH-R}	Receiver Input Threshold Voltage	Driver disabled	–30		30	mV
V_{TH-CB}	Cable Bias Detect Threshold, XTPBx Cable Inputs	Driver disabled	0.6		1.0	V
V_{TH+}	Positive Arbitration Comparator Threshold Voltage	Driver disabled	89		168	mV
V_{TH-}	Negative Arbitration Comparator Threshold Voltage	Driver disabled	–168		–89	mV
$V_{TH-S200}$	S200 Speed Signal Threshold	Driver disabled	49		131	mV
$V_{TH-S400}$	S400 Speed Signal Threshold	Driver disabled	314		396	mV
I_{CD}	Connect Detect Output at TPBIAS Pins				76	μA

1394 PHY Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
	Power Status Threshold	CPS input with 1k/11k voltage divider	7.8	40	V
	TPBIAS Output Voltage	At I_O current	1.665	2.015	V

10 Mechanical Specification



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	7.00 BSC			0.276 BSC		
D1/E1	6.75 BSC			0.266 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
Θ	0°	---	14°	0°	---	14°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

Exposed Pad Size						
L / F	D2/E2 (mm)			D2/E2 (inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
	4.90	5.05	5.20	0.193	0.199	0.205

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

Figure 5 – VT6315N QFN-48 Package (7 mm×7 mm)

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