Data Sheet

VT6105M

Rhine III 10/100 Mbps PCI Fast Ethernet Controller with ACPI and Management Functions

Preliminary Revision 1.0
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VIA TECHNOLOGIES, INC.

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Rhine III

10 / 100 Mbps PCI Fast Ethernet Controller
with ACPI and Management Functions

PRODUCT FEATURES

- **Single Chip Fast Ethernet Network Interface Controllers (NICs) for the PCI Bus**
  - PCI 2.2 specification compliant
  - Provide a direct connection to the PCI bus
  - Support 10 / 100 Mbps ethernet communications with BootROM interface
- **High Performance PCI Mastering Structure**
  - VIA-defined 256 byte I/O-based or memory-mapped-I/O-based command and status registers
  - Software oriented chain structure description to minimize hardware complexity
  - On chip bus master DMA with programmable burst length for high PCI bus utilization
  - Transmit data buffer byte-alignment for low CPU utilization
  - Dynamic transmit packet auto-queuing for back-to-back transmission
  - Programmable activity polling intervals for description DMA
  - Programmable DMA arbitration priority to minimize overflow under flow conditions
  - Early receive and early transmit interrupts for software parallel processing
  - Interrupt controllable by receive/transmit descriptor list for saving interrupt service time
  - PCI enhance command capable
- **Provides Standard 10 Base-T / 100Base-Tx/Fx PHY Layer and Transceiver**
  - Supports 10 Base-T / 100Base-TX / FX with CAT5 UTP, STP and fiber cables
  - 10 / 100 Mbps full duplex, half duplex operation
  - Auto MDI / MDIX functions N-Way enable or PHY force-media mode
  - Auto Power-saving at cable not link
  - Four LED outputs, including Link, Duplex, Speed, and Collision status
- **Separate 2K Bytes FIFO for Receive and Transmit Controllers**
  - Both support bursts of up to full Ethernet length
  - Programmable receive and transmit FIFO threshold control for optimize PCI throughput
- **Flexible Dynamic-Load EEPROM Algorithm**
  - Load after power-up
  - Dynamic auto reload
  - Embedded programming for configuration modification
  - Dynamic direct programming for manufacturing
- **External Boot ROM**
  - Up to 64K Bytes
  - No external address latch required
  - Supports EPROM read and Flash ROM read / write

- **ACPI**
  - Supports PC99, PC2001 and Net PC requirements
  - Supports PCI Bus Power Management Interface Specification Version 1.0 / 1.1
  - Supports Advanced Configuration and Power Interface (ACPI) Specification 1.0
  - Supports Network Device Class Power Management Specification Version 1.0a
  - Wake-up even support link change / magic packet / unicast physical address / MS define pattern match
- **Flow Control**
  - Supports IEEE 802.3X for full duplex
  - Multiple pause frame XON / XOFF
- **MAC Enhancement Function for Management Server NICs**
  - IEEE 802.1p priority transmit, programmable (by driver) maximum of eight priority queues
  - IEEE 802.1q multiple VLAN with VLAN ID auto insertion / extraction and VID filtering support
  - UDP, TCP/IP checksum offload for IPv4 frames
  - Statistics of 12 sets of hardware Management Information Base counters
  - Unicast, broadcast, and multicast address filtering hashing table
  - 32 sets Multicast / interesting packet perfect-filtering
  - 32 sets VLAN ID perfect-filtering
- **Full Software Support to Network OS**
  - Windows 95, (including OSR2), Windows 98, Windows 98 (including SE, Windows ME, Win2000, Windows XP, Word for Workgroups 3.11, Windows NT 3.51 and 4.0
  - LAN Manager, LANtastic, PC-NFS
  - NCSA Telnet
  - Novell Netware 3.11, 3.12, 4.x, 5.x, 6.0, Client 32, Netware Client
  - RedHat Linux 6.2, 7.0,7.1
  - FreeBSD 3.2, 4.0, 4.11, 4.2
  - UnixWare 8.0, SCO UNIX 5.0
- **Management Feature Software Support**
  - Install Parameter Setting
  - Statistics Monitor
  - Diagnostic utility to test VT6105M functions
  - VLAN Manager
  - NIC teaming (LBFO) management
  - RMON Group 1.2.39
- **Utilities**
  - Windows auto installation, Utility for MS-DOS diagnostics
  - Desktop Management Interface (DMI) 2.0
  - BootBios support for Flash update, Remote Program Load booting to MS-DOS, and Windows 95
  - Preboot Execution Environment
- **Dual Power Design: 3.3V I/O Power and 2.5V Core Power**
- **0.22um TSMC CMOS Technology**
- **128-Pin PQFP Package**

OVERVIEW

The VIA Rhine III Fast Ethernet controllers are cutting edge, feature-rich, and cost-competitive single ASIC chip solutions for PC NIC adapters (VT6105) and PC Server NIC adapters (VT6105M). The VT6105M is a high-performance network solution for workstations and servers, offering 200 Mbits per second aggregate bandwidth in full duplex mode, easing server processor utilization by optimizing throughput between the NIC and the PCI bus without using the system CPU. Arange of critical performance and advanced management-related features are supported including 802.1p priority transmissions, TCP/IP checksum offload, multiple VLANs, IEEE 802.3x flow control and adaptive interrupts.

Rhine III controllers feature extensive troubleshooting features including auto MDI / MDIX configuration and remote BootROM ability. Advanced power management features (fully compliant with PCI Power Management Revision 1.1 and ACPI Revision 1.0) are also available for low power consumption. Wake on LAN (WOL) allows multiple wake-up events including magic pckets, pattern matching packets and link status changes. The VT6105M is designed with advanced 0.22 micron CMOS process technology for low power.

The VT6105M is ideal for integration into network controllers, network workstations, NICs, or LAN-on-motherboard solutions, providing a manageable, integrated controller to bring high speed Ethernet connectivity to the electronics of tomorrow. The driver and silicon were developed together, resulting in optimal performance in terms of both throughput and host CPU utilization.

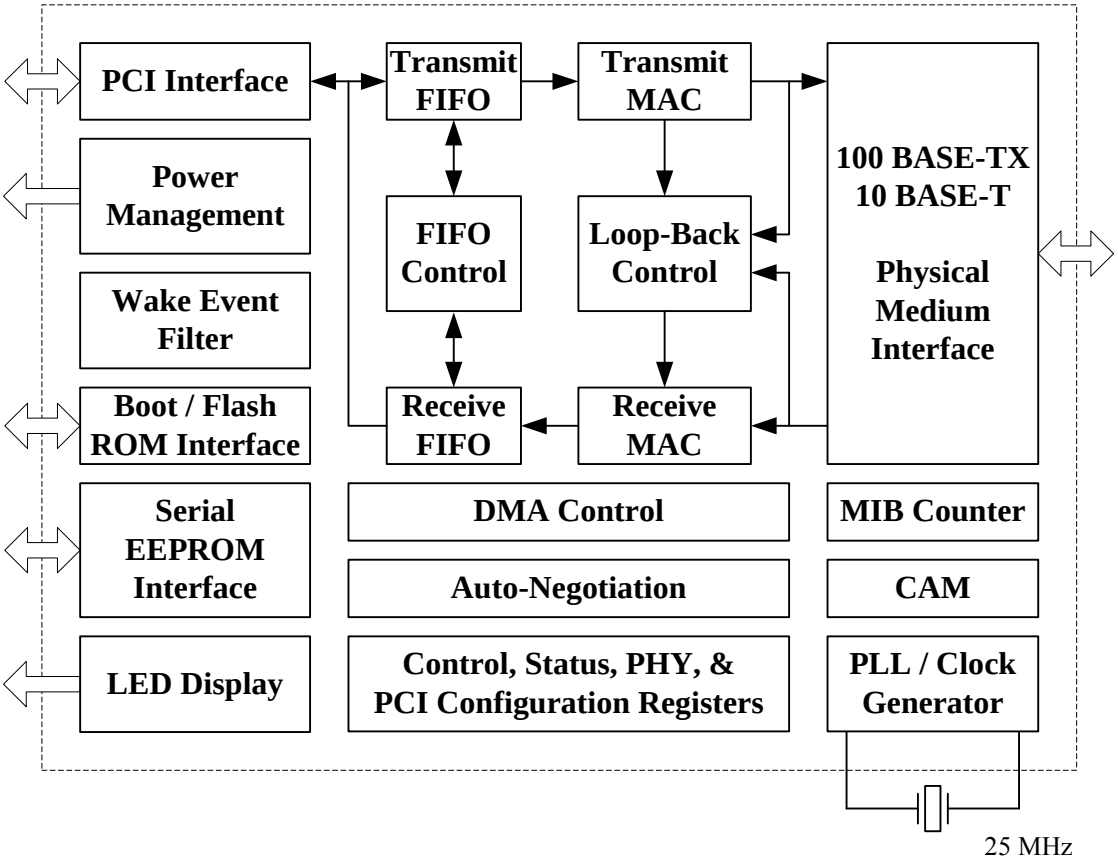


Figure 1. Internal Block Diagram

PINOUTS

Pin Diagram

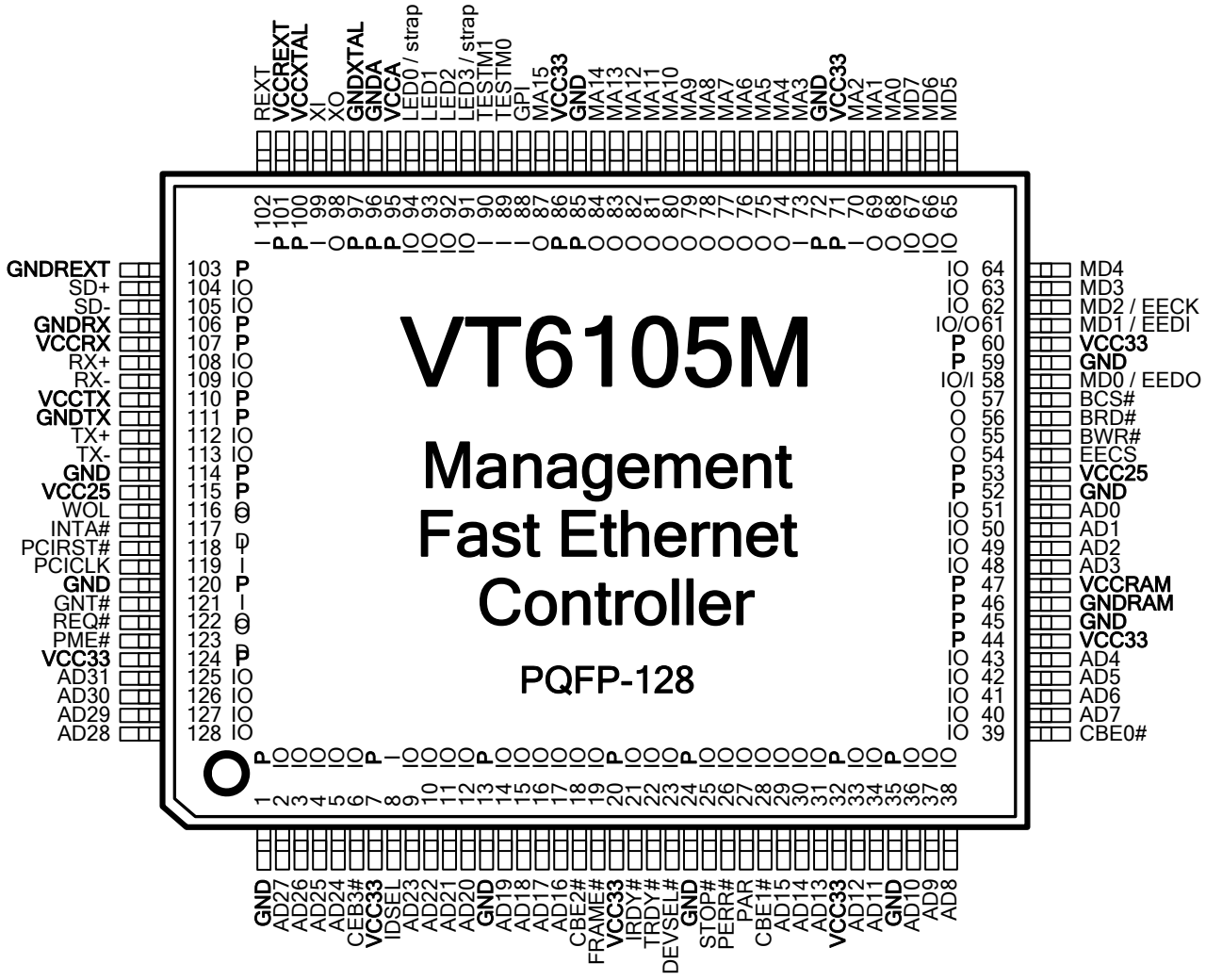


Figure 2. Pin Diagram

Pin List

Table 1. Pin List

Pin Name	Pin #	Type	Pin Name	Pin #	Type	Pin Name	Pin #	Type	Pin Name	Pin #	Type
AD00	51	I/O	BPCS#	57	O	LED0 / strap	94	IO	PME#	123	OD
AD01	50	I/O	BPRD#	56	O	LED1	93	IO	REQ#	122	O
AD02	49	I/O	BPWR#	55	O	LED2	92	IO	REXT	102	I
AD03	48	I/O	CBE0#	39	I/O	LED3 / strap	91	IO	RX+	108	I/O
AD04	43	I/O	CBE1#	28	I/O	MA0	68	O	RX–	109	I/O
AD05	42	I/O	CBE2#	18	I/O	MA1	69	O	SD+	104	I
AD06	41	I/O	CBE3#	6	I/O	MA2	70	I	SD–	105	I
AD07	40	I/O	DEVSEL#	23	I/O	MA3	73	I	STOP#	25	I/O
AD08	38	I/O	EECS	54	O	MA4	74	O	TESTM0	89	I
AD09	37	I/O	FRAME#	19	I/O	MA5	75	O	TESTM1	90	I
AD10	36	I/O	**GND**	**1**	**P**	MA6	76	O	TRDY#	22	I/O
AD11	34	I/O	**GND**	**13**	**P**	MA7	77	O	TX+	112	I/O
AD12	33	I/O	**GND**	**24**	**P**	MA8	78	O	TX–	113	I/O
AD13	31	I/O	**GND**	**35**	**P**	MA9	79	O	**VCC25**	**53**	**P**
AD14	30	I/O	**GND**	**45**	**P**	MA10	80	O	**VCC25**	**115**	**P**
AD15	29	I/O	**GND**	**52**	**P**	MA11	81	O	**VCC33**	**7**	**P**
AD16	17	I/O	**GND**	**59**	**P**	MA12	82	O	**VCC33**	**20**	**P**
AD17	16	I/O	**GND**	**72**	**P**	MA13	83	O	**VCC33**	**32**	**P**
AD18	15	I/O	**GND**	**85**	**P**	MA14	84	O	**VCC33**	**44**	**P**
AD19	14	I/O	**GND**	**114**	**P**	MA15	87	O	**VCC33**	**60**	**P**
AD20	12	I/O	**GND**	**120**	**P**	MD0 / EEDO	58	IO/I	**VCC33**	**71**	**P**
AD21	11	I/O	**GNDA**	**96**	**P**	MD1 / EEDI	61	IO/O	**VCC33**	**86**	**P**
AD22	10	I/O	**GNDRAM**	**46**	**P**	MD2 / EECK	62	I/O	**VCC33**	**124**	**P**
AD23	9	I/O	**GNDREXT**	**103**	**P**	MD3	63	I/O	**VCCA**	**95**	**P**
AD24	5	I/O	**GNDRX**	**106**	**P**	MD4	64	I/O	**VCCRAM**	**47**	**P**
AD25	4	I/O	**GNDTX**	**111**	**P**	MD5	65	I/O	**VCCREXT**	**101**	**P**
AD26	3	I/O	**GNDXTAL**	**97**	**P**	MD6	66	I/O	**VCCRX**	**107**	**P**
AD27	2	I/O	GNT#	121	I	MD7	67	I/O	**VCCTX**	**110**	**P**
AD28	128	I/O	GPI	88	I	PAR	27	I/O	**VCCXTAL**	**100**	**P**
AD29	127	I/O	IDSEL	8	I	PCICLK	119	I	WOL	116	O
AD30	126	I/O	INTA#	117	OD	PCIRST#	118	I	XO	98	O
AD31	125	I/O	IRDY#	21	I/O	PERR#	26	I/O	XI	99	I

Pin Descriptions

Table 2. Pin Descriptions

PCI Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AD[31:0]	(see pin list)	I/O	**Address and Data.** Address and data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. In the data phase of the clock cycle IRDY# and TRDY# are both asserted. Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted.
CBE#[3:0]	6, 18, 28, 39	I/O	**Bus Command / Byte Enable.** These commands are multiplexed on the same PCI pins. During the address phase of a transaction, CBE#[3:0] defines the Bus Command. During the data phase, CBE#[3:0] uses the Byte Enable command. The Byte Enables define which physical byte lanes on the bus carry the data. CBE#[0] applies to byte 0 and CBE#[3:0] applies to byte 3.
PAR	27	I/O	**Parity.** Even parity across AD[31-0] and CBE#[3-0]. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction.
IDSEL	8	I	**Initialization Device Select**. Used as a chip select during PCI configuration read and write-cycles.
FRAME#	19	I/O	**Frame.** Cycle Frame is driven by the current bus master to indicate the address stage that marks the beginning and duration of a bus transaction. During the address stage the FRAME# is asserted low to indicate that a bus transaction is beginning. While the FRAME# is asserted, data transfers continue. When the FRAME# is negated, the transaction is in the final data phase.
DEVSEL#	23	I/O	**Device Select**. When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
IRDY#	21	I/O	**Initiator Ready.** Indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a write cycle, IRDY# indicates that transferring data is present on AD[31:0]. During a read cycle, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
TRDY#	22	I/O	**Target Ready.** Indicates the target agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a read, TRDY# indicates that valid data is present on AD31-0. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
STOP#	25	I/O	**Stop.** The VT6105M drives STOP# to discontinue further action.
PERR#	26	I/O	**Parity Error.** Asserts when a data parity error is detected.
REQ#	122	O	**Bus Request.** Asserted by the VT6105M indicate to the PCI bus arbiter that it wants to use the bus for bus master operations.
GNT#	121	I	**Bus Grant.** Asserts to indicate to the VT6105M that access to the bus is granted.
INTA#	117	OD	**Interrupt.** An asynchronous signal used to request an interrupt
PCICLK	119	I	**PCI Clock.** Provides timing for all transactions on the PCI bus and is an input pin to every PCI device.
PCIRST#	118	I	**PCI Reset.** When PCIRST# is asserted low, the VT6105M chip performs an internal system hardware reset. PCIRST# may be asynchronous to PCICLK when asserted or negated, but it is recommended that the negation be synchronous to guarantee a clean and bounce-free signal edge.

Boot ROM / EEPROM Interface

Signal Name	Pin #	I/O	Signal Description
MA[15:0]	(see pin list)	O	**Boot ROM Address.** MA2 and MA3 are also used as power-up straps: **MA2.** PHY: MDI / MDIX function disable when pull up, default is enable. **MA3.** Must be pulled up with 10k external resistor for normal operation.
BPWR#	55	O	**Boot ROM Write Enable.** Used to write to the Boot ROM if it is writable (flash).
BPRD#	56	O	**Boot ROM Read Enable.** Used to read Boot ROM data on the memory data bus.
BPCS#	57	O	**Boot ROM Chip Select.** Used to select the Boot ROM for a read or write.
MD7	67	IO	**Boot ROM Data Bus / Serial EEPROM Control.**
MD6	66	IO	
MD5	65	IO	
MD4	64	IO	
MD3	63	IO	
MD2 / EECK	62	IO / O	EECK = Serial EEPROM Clock.
MD1 / EEDI	61	IO / O	EEDI = Serial EEPROM Data In.
MD0 / EEDO	58	IO / I	EEDO = Serial EEPROM Data Out.
EECS	54	O	**Serial EEPROM Chip Select.** Chip select signal for an external serial EEPROM when an EEPROM is used to provide the configuration data and Ethernet Address.

LED Interface

Signal Name	Pin #	I/O	Signal Description
LED3 / strap **LED2** **LED1** **LED0** / strap	91 92 93 94	O / I O O O / I	**LED Identification.** LED displays for network traffic status identification. The LED select bits in PHY register Rx10 can be used to set the LED definitions. The default LED definitions are: LED0: Link/Act LED1: Speed LED2: Duplex LED3: Collision The LED0 and LED3 pins are also used as power-up straps: Need external resistor to pull up or pull down. LED0 strap = Test Mode (0 = Internal PHY test mode, 1 = normal operation) LED3 strap = N-Way Enable (0 = disable, 1 = enable)

Power Management Interface

Signal Name	Pin #	I/O	Signal Description
WOL	116	O	**Wake on LAN Event.** Active high, programmable pulse or button WOL event
PME#	123	OD	**Power Management Event**. Power management interrupt output

Physical Cable Connection

Signal Name	Pin #	I/O	Signal Description
TX+, TX–	112,113	IO	**Differential Transmit Pair.** 10/100 Base – T/TX and 100 Base Fx transmit data
RX+, RX–	108,109	IO	**Differential Receive Pair.** 10/100 Base – T/TX and 100 Base Fx receive data
SD+, SD–	104,105	I	**Differential Signal Detect.** On 100 Base FX (no fiber mode), TP mode must be tied to GND directly.

Clocks, Control and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
XI	99	I	**Crystal In.** Connect to 25 MHz crystal with (22pF 5%) pF capacitor connection to GNDOSC. Can alternately be driven by an external clock source (3.3V voltage swing) with XO unconnected.
XO	98	O	**Crystal Feedback.** Connect to other side of 25 MHz crystal and to 22pF 5% GNDOSC capacitor.
REXT	102	I	**External Resistor.** Connect 6.04 KΩ 1% resistor to GND.
GPI	88	I	Connect to PCI power to detect PCI power status for Wake on LAN usage. Must be pulled up to PCI5V with a 10 KΩ resistor.
TESTM0	89	I Pull Low	**Test and Operation Mode Select 0.** (For internal use)
TESTM1	90	I Pull Low	**Test and Operation Mode Select 1.** (For internal use)

Digital Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC33	86, 71, 60, 44, 32, 20, 7, 124	P	**I/O Power.** +3.3V ±5%
VCC25	115, 53	P	**Core Power.** +2.5V ±5%
GND	1, 13, 24, 35, 45, 52, 59, 72, 85, 114, 120	P	**Digital Ground.** Connect directly to main PCB ground plane.
VCCRAM	47	P	**Power for Internal FIFO SRAM.** +2.5V ±5%
GNDRAM	46	P	**Ground for Internal FIFO SRAM.** Connect directly to main PCB ground plane.

Analog Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCA	95	P	**Analog Power.** 2.5V ±5% power for internal analog circuitry.
GNDA	96	P	**Analog Ground.** Connect to analog ground.
VCCTX	110	P	**PHY Transmitter Power.** 2.5V ±5% power for internal PHY transmitter circuitry.
GNDTX	111	P	**PHY Transmitter Ground.** Connect to analog ground.
VCCRX	107	P	**PHY Receiver Power.** 2.5V ±5% power for internal PHY receiver circuitry.
GNDRX	106	P	**PHY Receiver Ground.** Connect to analog ground.
VCCREXT	101	P	**External Resistor Circuit Power.** 2.5V ±5% power for internal analog circuitry associated with the external resistor REXT.
GNDREXT	103	P	**External Resistor Circuit Ground.** Connect to analog ground.
VCCXTAL	100	P	**Crystal Oscillator Power.** 2.5V ±5% power for internal crystal oscillator circuit.
GNDXTAL	97	P	**Crystal Oscillator Ground.** Connect to analog ground.

REGISTERS

Register Overview

The tables in this section describe the register settings for the VT6105M. The registers in this section are listed according to their offset values. The tables show the Access Type (Read/Only, Read/Write, and Read/Write/Clear) and power-on default values ("Default). All offset values are shown in hexadecimal unless otherwise indicated. Default values for each register are also indicated in hexadecimal notation.

Note: Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers assigned as RWC or WC may have some read-only or read-write bits (see individual register descriptions for details)

Register Summary

Table 3. Register Summary Tables

PCI Configuration-Space Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3053**	RO
5-4	Command	**0097**	**RW**
7-6	Status	**0210**	RO
8	Revision ID	**nn**	RO
B-9	Class Code	02 00 00	RO
C	Cache Line Size	08	**RW**
D	Latency Timer	40	**RW**
E	Header Type	00	RO
F	BIST	00	RO
13-10	IO Base Address	00 00 D8 01	RO
17-14	MEH Base Address	F6 80 00 00	RO
2B-18	-reserved	—	—
2D-2C	Sub Vender ID	1106	RO
2F-2E	Sub System ID	0106	RO
33-30	Expansion ROM Base Address	—	RW
34	Capability Pointer	**40**	RO
3B-35	-reserved-	00	RO
3C	Int Line	—	RO
3D	Int Pin	—	RO
3E	Min_GNT	3	RO
3F	Max_LAT	8	RO
40	Cap ID	1	RO
40-35	-reserved-	00	—
41	Next Item Pointer	00	RO
43-42	Power Management Event	00	RO
4F-44	Power Management Ctrl / Status		**RWC**
FF-50	-reserved-	00	—

Internal Registers (00h-FFh)

Offset	Control / Status / Interrupts	Default	Acc
5-0	MAC Address 0-5 (PAR 0-5)	6 x 00	RW
6	Receive Control (RCR)	0	RW
7	Transmit Control (TCR)	0	RW
8	Command 0 (CR0)	04	RW
9	Command 1 (CR1)	08	RW
A	Transmit Queue Wake	00	RW
B	-reserved-	00	—
C	Interrupt Service 0 (ISR0)	—	RWC
D	Interrupt Service 1 (ISR1)	00	RWC
E	Interrupt Enable Mask 0 (IMR0)	0	RW
F	Interrupt Enable Mask 1 (IMR1)	0	RW
17-10	Multicast Hashing Table 0-7 (MAR0-MAR7) / CAM Data Port	8x FF	RW
1B-18	Rx Queue Descriptor Base Address	0	RW
1F-1C	Tx Queue 7 Descriptor Base Addr	0	RW
23-20	Tx Queue 6 Descriptor Base Addr	0000 0000	RW
27-24	Tx Queue 5 Descriptor Base Addr	0000 0000	RW
2B-28	Tx Queue 4 Descriptor Base Addr	0000 0000	RW
2F-2C	Tx Queue 3 Descriptor Base Addr	0000 0000	RW
33-30	Tx Queue 2 Descriptor Base Addr	0000 0000	RW
37-34	Tx Queue 1 Descriptor Base Addr	0000 0000	RW
3B-38	Tx Queue 0 Descriptor Base Addr	0000 0000	RW
6B-3C	Test (Do Not Program)	00	—

Offset	Media Independent Interface	Default	Acc
6C	MII Configuration (MII_CFG)	01	RW
6D	MII Status (MII_SR)	13	RW
6E	Bus Control 0 (BCR0)	09	RW
6F	Bus Control 1 (BCR1)	0E	RW
70	MII Control (MII_CR)	0	RW
71	MII Port Address (MII_PA)	81	RW
73-72	MII R/W Data Port (MII_RWDR)	7849	RW

Internal Registers (continued)

Offset	ROM / Chip Config / Misc	Default	Acc
74	EEPROM Ctrl / Status (EECSR)	80	RW
78	Chip Configuration A (CFG_A)	12	RW
79	Chip Configuration B (CFG_B)	00	RW
7A	Chip Configuration C (CFG_C)	40	RW
7B	Chip Configuration D (CFG_D)	82	RW
7F-7C	-reserved-	00	—
81-80	Misc Command (MCR0-1)	0000	RW
82	PM Capability Control (PMCCR)	1F	RW
83	Sticky Bit H/W Shadow (SBHS)	00	RW

Offset	Interrupt / CAM	Default	Acc
84	Misc Interrupt Status (MISR)	00	RWC
86	Misc Int Ena Mask (MIMR)	0	RW
8B-88	CAM Enable Mask (CAMMSK)	4x 00	RW

Offset	Flash / ROM Control	Default	Acc
8D-8C	Flash Programming Address	0000	RW
8E	Test (Do Not Program)	00	—
8F	Flash ROM Data	00	RW
90	Flash Command	80	RW
91	Flash Read Data	00	RW

Offset	Content Addressable Memory	Default	Acc
92	CAM Control	00	RW
93	CAM Control	00	RW

Offset	MIB / ANAR / Flow Ctl / Timer	Default	Acc
94	MIB Counter Control (MIBCR)	10	RW
95	PHY ANAR (ANAR)	00	RW
97-96	MIB Counter Data (MIBDAT)	0000	**RO**
98	Flow Control 0 (FCR0)	0	RW
99	Flow Control 1 (FCR1)	00	RW
9B-9A	Transmit Pause Frame Timer	0000	RW

Offset	Wake-On LAN (WOL)	Default	Acc
A4/A0	WOL Command Set / Clear	00/00	**RWC**
A5/A1	Power Configuration Set / Clear	10/10	**RWC**
A6/A2	Test (Do Not Program)	04/04	—
A7/A3	Wake-Up LAN Control	00/00	**RWC**
AC/A8	WOL Status 0	00/00	**RWC**
AD/A9	WOL Status 1	00/00	**RWC**
AE/AA	-reserved-	00/00	—
AF/AB	-reserved-	00/00	—

Offset	CRC / Byte Mask	Default	Acc
BF-B0	CRC Pattern 0-3 (CRC0-3)	16 x FF	RW
CF-C0	Byte Mask 0	16x 00	RW
DF-D0	Byte Mask 1	16x 00	RW
EF-E0	Byte Mask 2	16x 00	RW
FF-F0	Byte Mask 3	16x 00	RW

PHY Registers (00h-1Fh)

Offset	Internal Registers	Default	Acc
0	PHY Control	**3100**	RW
1	PHY Status	**7849**	**RO**
2	PHY Identifier 0	**0101**	**RO**
3	PHY Identifier 1	**8F43**	**RO**
4	Auto-Negotiation Base Page Advertisement	**05E1**	RW
5	Auto-Negotiation Link Partner Base Page Ability	0000	**RO**
6	Auto-Negotiation Expansion	**0005**	**RO**
7	Auto-Negotiation Next Page Transmit	**0000**	RW
8	Auto-Negotiation Link Partner Received Next Page	0000	**RO**
F-9	-reserved-	—	—
10	PHY Configuration 1	**0800**	RW
11	PHY Configuration 2	**F7FF**	RW
12	PHY Configuration 3	**0800**	RW
13	PHY Interrupt Mask	**FFFC**	RW
14	PHY Status	7003	**RO**
18-15	Reserved (Do Not Program)	—	—
19	Power Control	0001	RW
1F-1A	Reserved (Do Not Program)	—	—

Register Descriptions

PCI Configuration-Space Registers

Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (3053h) ..... RO

15-0 ID Code (reads 3053h to identify the VT6105M)

Offset 5-4 - Command (0006h) ..... RW

15-10 Reserved ..... always reads 0
9 Fast Back-to-Back Enable ..... always reads 0
8 SERR# Enable ..... always reads 0
7 Wait Cycle Control ..... always reads 0
6 Parity Error Response ..... always reads 0
5 VGA Palette Snoop ..... always reads 0
4 Memory Write & Invalidate Enable always reads 0
3 Special Cycles Enable ..... always reads 0
2 PCI Bus Master Enable ..... always reads 0
1 Memory Space Enable ..... always reads 0
0 I/O Space Enable ..... always reads 0

Offset 7-6 - Status (0290h) ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signaled System Error ..... always reads 0
13 Received Master Abort ..... always reads 0
12 Received Target Abort ..... always reads 0
11 Signaled Target Abort ..... always reads 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... **always reads 01**
10 Slow
11 Reserved
8 Data Parity Error Detected ..... always reads 0
7 Fast Back-to-Back Capable ..... **always reads 1**
6 User Definable Features ..... always reads 0
5 66 MHz Capable ..... always reads 0
4 Power Management Capabilities ..... **always reads 1**
3-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Revision ID ..... always readscurrent revision #

Offset B-9 - Class Code ..... RO

Identifies the generic function of the device and specific register-level programming interfaces.

31-8 Class Code ..... default = 00 00 00h

Offset C - Cache Line Size ..... RW

Implemented by master devices that are able to generate the memory write command as well as the memory invalidate command.

7-0 Cache Line Size ..... default = 00h

Offset D - Latency Timer ..... RW

Implemented as write able by a master device that can burst more than two data phases.

7-0 Latency Timer ..... default = 00h

Offset E - Header Type ..... RO

Refer to the PCI version 2.1 Specification.

7-0 Header Type ..... default = 00h

Offset F - Built In Self Test (BIST) (00h) ..... RO

7-0 BIST ..... default = 00h

Offset 34 - Capability Pointer ..... RO

Provides an offset into the function's PCI configuration space for the location of the first item in the Capabilities linked list

7-0 Capability Pointer ..... default = 00h

Offset 41 - Next Item Pointer ..... RO

Provides an offset into the function's PCI configuration space pointing to the location of the next item in the function's capability list

7-0 Next Item Pointer ..... default = 00h

Offset 43-42 - Power Management Event ..... RO

15-11 PME_Supp ..... **RO**
This 5 bit field indicates the power state in which the function may assert PME#.
1xxxx PME# can be asserted from D3cold
x1xxx PME# can be asserted from D3hot
xx1xx PME# can be asserted from D2
xxx1x PME# can be asserted from D1
xxxx1 PME# can be asserted from D0
10-0 Reserved ..... always reads 0

Offset 4F - 44- Power Management Control Status ....RWC

Refer to Power Management spec 1.0.

Internal Registers (00-FFh)

Ethernet Address and Receive / Transmit Control

Offset 5-0 - Ethernet Address ..... RW

63-0 Ethernet Address PAR0-PAR5
Loaded from EEPROM at power up

Offset 6 - Receive Configuration Request ..... RW

7-5 Receive FIFO Threshold
- 000 64 byte..... default
- 001 32 byte
- 010 128 byte
- 011 256 byte
- 100 512 byte
- 101 768 byte
- 110 1024 byte
- 111 store & forward

4 Physical Address Packets Accepted
- 0 Physical address must match node address in PAR0-5.
- 1 All packets with physical destination address are accepted

3 Broadcast Packets Accepted
- 0 Packets with broadcast address are rejected
- 1 Packets with broadcast address are accepted

2 Multicast Packets Accepted
- 0 Packet with multicast are rejected
- 1 Packets with multicast address hit hashing table defined by MAR0-MAR7 are accepted

1 Runt Packets Accepted
- 0 Packets smaller than 64 bytes are rejected.
- 1 Packets smaller than 64 bytes are accepted.

0 Error Packets Accepted
- 0 Reject Packets with CRC error
- 1 Accept Packets with CRC error

Offset 7 - Transmit Configuration Request ..... RW

7-3 Reserved ..... RO

2-1 Transmit Loopback Mode
- 00 Normal
- 01 Internal loopback (MAC only)
- 1x Reserved

0 802.1P/Q Transmit Packet Tagging
- 0 Disable (transmit all packets untagged)
- 1 Enable (transmit all packets tagged)

Offset 8 - Control 0 ..... RW

7-5 Reserved ..... always reads 0

4 Transmit Process
- 0 Transmit state disabled ..... default
- 1 Transmit DMA state enabled

3 Receive Process
- 0 Receive state disabled ..... default
- 1 Receive DMA state enabled

2 Stop NIC
- 0 Command processing is in process
- 1 Shut down NIC operation ..... default

1 Start NIC
- 0 Command not entered. ..... default
- 1 Enable NIC operation

0 Reserved R0

Offset 9 - Control 1 ..... RW

7 Software Reset
- 0 Normal condition ..... default
- 1 Software reset (cleared after reset complete)

6 Receive Poll Demand ..... Self Clearing
- 0 Toggle bit…… ..... default
- 1 Set 1 to poll the RD once. It will be cleared automatically after polling is completed.

5 Transmit Poll Demand ..... Self Clearing
- 0 Toggle bit ..... default
- 1 Set 1 to poll the TD once, it will be cleared by itself after polling complete.

4 Reserved ..... always reads 0

3 Disable TD/RD Auto Polling
- 0 Set TX/RX auto-polling enable
- 1 Set TX/RX auto polling disable ..... default

2 Full Duplex
- 0 Set MAC to half duplex mode ..... default
- 1 Set MAC to full duplex mode

1 Disable Accept Unicast Packet
- 0 Accept the incoming packet destined to the VT6105M MAC Address…… ..... default
- 1 Reject the incoming packet destined to the VT6105M MAC Address

0 Reserved ..... RO

Offset A – Transmit Queue Wake ..... RW

7-0 Transmit Queue Append Indicator
(set by software but cleared by hardware)

Interrupt Control

Offset 0C – Interrupt Status 0 .....RW

- **7** **MIB Counter Overflow** ..... default = 0
- **6** **PCI Bus Error** ..... default = 0
- **5** **Receive Descriptor Linking Error** ..... default = 0
- **4** **Transmit Descriptor Structure Error** .... default = 0
- **3** **Transmit Error**
  - 0 Packet transmission with no errors .....default
  - 1 Packet transmission is aborted due to
    - FIFO Underflow
    - Excessive collisions
    - PCI Bus error
    - TD structure error
- **2** **Receive Error**
  - 0 Packets received with no errors .....default
  - 1 Packet received with the following errors:
    - FIFO Overflow
    - CRC error
    - Frame alignment error
    - RD structure error
- **1** **Packet Transmitted Successfully** ..... default = 0
- **0** **Received Packet Successful** ..... default is 0

Offset 0D – Interrupt Status 1 .....RW

- **7** **General Purpose Interrupt** ..... default = 0
- **6** **Port State Change** ..... default = 0
- **5** **Excessive Collisions (Transmit Abort)** ... default = 0
- **4** **RD running up** ..... default is 0
- **3** **Receive FIFO Queue List Overflow** ..... default = 0
- **2** **Receive FIFO Overflow** ..... default = 0
- **1** **Transmit FIFO Underflow Event** ..... default = 0
- **0** **Early Receive Interrupt** ..... default = 0

Offset 0E - Interrupt Mask 0 (00h) .....RW

All bits correspond to the bits in the Interrupt Status 0 register.

Offset 0F - Interrupt Mask 1 (00h).....RW

All bits correspond to the bits in the Interrupt Status 1 register.

Multicast Address / CAM Data

Offset 17 – 10 - Multicast Address / CAM Data Port.... RW

- **63-0** **Multicast Address Hash Table MAR[7-0]**

- **63-48** **VID_CAM**
- **47-0** **Multi_CAM**

Transmit / Receive Descriptor Base Addresses

Offset 1B - 18 – Receive Descriptor Base Address.....RW

31-0 Receive Descriptor List Start Address

Offset 1F-1C – Queue 7 Transmit Descriptor Base Address .....RW

31-0 Queue 7 Transmit Descriptor List Start Address

Offset 23 - 20– Queue 6 Transmit Descriptor Base Address .....RW

31-0 Queue 6 Transmit Descriptor List Start Address

Offset 27-24 – Queue 5 Transmit Descriptor Base Address .....RW

31-0 Queue 5 Transmit Descriptor List Start Address

Offset 2B-28 – Queue 4 Transmit Descriptor Base Address .....RW

31-0 Queue 4 Transmit Descriptor List Start Address

Offset 2F-2C – Queue 3 Transmit Descriptor Base Address .....RW

31-0 Queue 3 Transmit Descriptor List Start Address

Offset 33-30 – Queue 2 Transmit Descriptor Base Address .....RW

31-0 Queue 2 Transmit Descriptor List Start Address

Offset 37-34 – Queue 1 Transmit Descriptor Base Address .....RW

31-0 Queue 1 Transmit Descriptor List Start Address

Offset 3B-38 – Queue 0 Transmit Descriptor Base Address .....RW

31-0 Queue 0 Transmit Descriptor List Start Address

MII Control

Offset 6C - MII Configuration (MII_CFG) ..... RW

7-6 MII Management Polling Timer Interval
- 00 1024 Management Data Clock cycles ... default
- 01 512 Management Data Clock cycles
- 10 128 Management Data Clock cycles
- 11 64 Management Data Clock cycles

5 Accelerate Management Data Clock Speed
- 0 Management Data Clock=normal..... default
- 1 Management Data Clock=4x accelerated

4-0 Extend PHY Device Address

PHY chip address for management port access. Can be programmed by software..... **default = 00001b**

Offset 6D – MII Status (MIISR) ..... RW

7 Software PHY Reset
- 0 De-asserted ..... default
- 1 Asserted

6 Asm_Pause Status after N-Way..... **RO**
..... default = 0

5 Pause Status after N-Way..... **RO**
..... default = 0

4 Link Status after N-Way ..... **RO**
- 0 Link successful ..... default
- 1 No cable connected

3 PHY Device Received Error..... **RO**
- 0 No error ..... default
- 1 Error

2 Duplex Mode after N-Way ..... **RO**
- 0 Half Duplex ..... default
- 1 Full Duplex

1 Link Status after MII Polling..... **RO**
- 0 Link successful ..... default
- 1 Link failed

0 Link Speed After N-Way..... **RO**
- 0 100 Mbps..... default
- 1 10 Mbps

Bus Control

Offset 6E – Bus Control 0 (BCR0).....RW

7-6 Reserved ..... always reads 0
5-3 Reserved ..... always reads 0
2-0 DMA Length
000 32 bytes (8 Double Words).....default
001 64 bytes (16 Double Words
010 128 bytes (32 Double Words)
011 256 bytes (64 Double Words)
100 512 bytes (128 Double Words)
101 1024bytes (256 Double Words)
11x Store & forward (flush till empty)

Offset 6F – Bus Control 1 (BCR1).....RW

7 VLAN ID Hardware Filtering
0 Disable .....default
1 Enable
6 Higher Transmit Queues Block Lower Ones
0 Blocked .....default
1 Not blocked
5-3 Reserved ..... always reads 0
2 Polling Time Interval 2..... **default is 1**
1 Polling Time Interval 1..... **default is 1**
0 Polling timer interval 0..... default is 0

MII Programming (PHY Read / Write Control)

Offset 70 – MII Control (MIICR) ..... RW

7 MII Management Port Auto Polling
0 Disable (bits 6-0 of this register are ignored) ..... default
1 Enable
6 PHY Read Enable .....**Self-Clearing**
0 Normal..... default
1 Initiate PHY Read (register offset is stored in Rx71, read data is stored in Rx72-73)
5 PHY Write Enable .....**Self-Clearing**
0 Normal..... default
1 Initiate PHY Write (register offset is stored in Rx71, data to be written is stored in Rx72-73)
4 Direct Programming Mode
0 Enable..... default
1 Disable (bits 6 and 5 are ignored)
3 MDIO Output Enable Indicator while in Direct Programming Mode
2 Direct Programming Status – MDO Management Port Data Out
1 Direct Programming Input – MDI Management Port Data In While Reading PHY Status
0 Direct Programming Status – MDC Management Port Clock

Offset 71 – MII Management Port Address..... RW

7 MII Idle..... RO
0 MII auto polling cycle
1 Not in MII auto polling cycle ..... default
6 MII Status Change Enable
0 Open the Pause Function of MII Polling Cycle Done (MDONE)..... default
1 Close the Pause Function of MDONE
5 MDONE
When MDIO Auto Polling Data is Ready, MII State of SM is at the End of an Auto Polling Cycle
4-0 MII Management Port Address...**default = 00001b**

Offset 73-72 - MII Port Read / Write Data ..... RW

15-0 PHY Data For Write or PHY Data From Read

EEPROM Control / Status

Offset 74 – EEPROM Control / Status (EECSR).....RW

7 **EEPROM Programmed Status** .....**RO**
A value of 73H indicates programmed
6 **Reserved** ..... always reads 0
5 **Dynamic Reload EEPROM Content**
4 **Direct Program EEPROM Mode**
3 **Direct Program EECS Chip Select Pin Status**
2 **Direct Program EECK Clock Pin Status**
1 **Direct Program EEDI Data In Pin Status**
0 **Direct Program EEDO Data Out Pin Status**.....**RO**

Chip Configuration

Offset 78 - Chip Configuration A (CFG_A)..... RW

Note: This register always reads 00h after power is on and loading starts.

7 **EEPROM Embedded & Direct Programming**
0 Disable..... default
1 Enable
6 **MII Option..... MIIOPT**
0 Without extension clock..... default
1 With extension clock.
5 **Include Tag Information in CRC Calculation Pattern Match**
0 Tag excluded during calculation
1 Tag included during calculation
4-3 **LED Select**

	LED0	LED1	LED2	LED3
00	Link/Act	Speed	Duplex	COL.... def
01	Pwr/TxAct	Link/RxAct	Speed	Duplex
10	Speed100	Speed10	Act	Duplex
11	Pwr/TxAct	Link/RxAct	Speed	COL

2 **Reserved** .....always reads 0
1 **Abnormal shut down wake up enable**
0 Disable
1 Enable……..... default
0 **Pre-ACPI wake up enable**
0 Disable……..... default
1 Enable

Offset 79 - Chip Configuration B (CFG_B) ..... RW

7 **Transmit Frame Queuing**
0 Enable..... default
1 Disable
6 **Data Parity Generation and Checking**
0 Enable..... default
1 Disable
5 **Memory Read Line Support**
0 Enable..... default
1 Disable
4 **Transmitting FIFO DMA Will Interleave to Receiving FIFO DMA after 32 DW Transaction**
3 **Arbitration Priority Select**
TX FIFO DMA will be interleaved to RX FIFO DMA after 32 DWord transaction
2 **Master Read Insert One Wait State 2-2-2-2**
0 Disable..... default
1 Enable
1 **Master Write Insert One Wait State 2-2-2-2**
0 Disable..... default
1 Enable
0 **Latency Timer**
0 Disable..... default
1 Enable

Offset 7A - Chip Configuration (CFG_C) .....RW

7 Reserved ..... always reads 0

6 Tie Unused Boot ROM Address MA High
- 0 Disable .....default
- 1 Enable

5 Delay Transaction During Boot ROM Read
- 0 Disable .....default
- 1 Enable

4 Reserved ..... always reads 0

3 Boot ROM Timing Select
- 0 Fast .....default
- 1 Slow

2-0 Boot ROM Size Select
- 000 No Boot ROM.....default
- 001 8K size
- 010 16K size
- 011 32K size
- 1xx 64K size

Offset 7B - Chip Configuration D (CFG_D).....RW

7 Memory Mapped IO Access
- 0 Disable
- 1 Enable **.....default**

6 Diagnostic Mode
- 0 Disable .....default
- 1 Enable

5 Tag Insertion on Snap-Frame
- 0 Tag inserted from 13th byte.....default
- 1 Tag inserted after Snap coded (21st byte)

4 Reserved for Test (Do Not Program). .... default = 0

3 Random Backoff Algorithm
- 0 Disable .....default
- 1 Enable

2-0 Reserved for Test (Do Not Program)..... default = 0

Miscellaneous Control

Offset 80 - Miscellaneous Control (CR0) ..... RW

7-5 Reserved .....always reads 0

4 Transmit Full-Duplex Flow Control
- 0 Disable..... default
- 1 Enable

3 Receive Full-Duplex Flow Control
- 0 Disable..... default
- 1 Enable

2 Half-Duplex Flow Control
- 0 Disable..... default
- 1 Enable

1 Timer 0 Suspend..... Write 0 to Clear
- 0 Software Timer 0 will continue to count
- 1 Software Timer 0 Timeout (set by hardware)

0 Software Timer 0 Count Enable ..... **RW**
- 0 Disable..... default
- 1 Enable

Offset 81 - Miscellaneous Control (CR1) ..... RW

7 Software Generated Suspend Reset
- 0 Disable..... default
- 1 Enable

6 Force Exit Software Stop Without Waiting For Safestate
- 0 Disable..... default
- 1 Enable

5 Reserved .....always reads 0

4 Power Management Unit Support Version 1.0
- 0 Disable..... default
- 1 Enable

3 Reserved .....always reads 0

2 Soft-Timer Resolution in Microseconds
- 0 Disable..... default
- 1 Enable

1 PHY Event Interrupt Enable
(interrupt passed through INTA#)
- 0 Disable..... default
- 1 Enable

0 Software Timer 1 Count Enable
- 0 Disable..... default
- 1 Enable

Offset 82 - Power Mgmt Capability Control (PMCC)... RO

7-0 EEPROM PM Capability Shadow ... **default = 1Eh**

Offset 83 – Sticky Hardware Control (STICKHW) .....RW

7-4 Reserved ..... always reads 0

3 Legacy WOL Status

0 Disable .....default

1 Enable

2 Legacy WOL Enable

0 Disable .....default

1 Enable

1 Sticky DS1_Shadow Read-Write by Software

0 Sticky DS0_Shadow Suspend Well DS Write Port

MII Interrut Control

Offset 84 – MISC Interrupt Status (MISR) ..... RW

7 Power Event Report in Test Mode

6 User Defined Host Driven Interrupt

5 User Defined Host Driven Interrupt

4 Suspend Well MII Polling Status Change Interrupt by Diagnosis Use

3 Reserved .....always reads 0

2 PHY Event Interupt
(enabled by Rx81[1])

1 Software Timer 1 Interrupt

0 Software Timer 0 Interrupt

Offset 86 – MISC Interrupt Mask (MIMR)..... RW

7 Power Event Report in Test Mode Mask

6 User Defined Host Driven Interrupt Mask

5 User Defined Host Driven Interrupt Mask

4 Suspend Well MII Polling Status Change Interrupt By Diagnosis Use Mask

3 TD Internal Error Interrupt Mask

2 PHY Event Interrupt Mask

1 Software Timer 1 Interrupt Mask

0 Software Timer 0 Interrupt Mask

CAM Mask

Offset 8B-88 - CAM Entries Enable Mask (CAMMSK) .....RW

31-0 **MAR CAM** (CAM Select Rx92[1] = 0)
VID CAM (CAM Select Rx92[1] = 1)

Note: Individual bits enable related CMA entries. No write operations may be performed when CAM Write Enable (Rx92[0]) is 0.

Flash Direct Programming Control

Offset 8D-8C - Flash Programming Address..... RW

15-0 **Flash ROM Embedded Programming Address**

Offset 8F - Flash Embedded Write Data Port ..... RW

7-0 **Flash ROM Embedded Write Data Port**

Offset 90 - Flash Control Status..... RW

7 **Flash Embedded Programming Complete**
0 Not Complete ..... default
1 Complete

6-2 **Reserved** .....always reads 0

1 **Flash Embedded Write Command**
0 Normal operation..... default
1 Initiate Write Command

0 **Flash Embedded Read Command**
0 Normal operation..... default
1 Initiate Read Command

Note: Bit 7 is set after the embedded command is completed. Write operations are not allowed in normal operation.

Offset 91 - Flash Read Data..... RW

7-0 **Flash ROM Embedded Read Data Port**

CAM Control

Offset 92 - Content Addressable Memory Control .....RW

7-4 Reserved ..... always reads 0

3 CAM Read ..... Self-Clearing
- 0 Normal .....default
- 1 Read from CAM

2 CAM Write ..... Self-Clearing
- 0 Normal .....default
- 1 Write to CAM

1 CAM Select
- 0 Select Multicast Address CAM entries ..default
- 1 Select Virtual LAN CAM entries

0 CAM Write Enable
- 0 Disable (CAM may not be written).....default
- 1 Enable (CAM may be written)

Offset 93 - Content Addressable Memory Address .....RW

7-5 Reserved ..... always reads 0

4-0 CAM Address

MIB Counter Control

Offset 94 - MIB Counter Control (00h)..... RW

Note: MIB = Management Information Base

7 Return MIB Pointer to 0

6 Increment MIB Counter Pointed to by MIB Select

5 MIB Counter Half Threshold
- 0 Issue interrupt when MIB Counter = C000h .... default
- 1 Issue interrupt when MIB Counter = 8000h

4 MIB Counter Enable
- 0 MIB counter idle ..... default
- 1 MIB counter enabled to count events

3-0 MIB Counter Select
- 0000 Rx No Buf
- 0001 Rx Error Packet (RUNT|LONG|CRCE|FAE|FOVF)
- 0010 Rx FCS Error (CRCE)
- 0011 Rx MSD Packet Error (FOV|RACE)
- 0100 Rx FA Error (FAE)
- 0101 Rx Frame Too Long (LONG)
- 0110 Rx IRL Error (length mismatch)
- 0111 Rx Bad Opcode (receive control frame with unsupported opcode)
- 1000 Rx Pause Frames
- 1001 Tx Pause Frames
- 1010 Tx SQE Error
- 1011 Rx Symbol Error (RXER)

PHY ANAR

Offset 95 – PHY ANAR .....RO

7 ANAR Enable
0 Disable ANAR function.....default
1 Enable ANAR loaded and re-auto

6 Asm Flow Control
5 Flow Control
4 100 T4
3 100TXF
2 100TX
1 10TF
0 10T

This register is loaded from EEPROM and can be read / write through either I/O space or the MII management port. When writing ANAR via I/O cycle, the data will be written through the PHY-map registers.

MIB Counter Data

Offset 97-96 - MIB Counter Data ..... RO

15-0 MIB Counter Data

The host reads the MIB values in sequence MIB0 through MIB11

Flow Control

Offset 98 - Flow Control 0 (CR0).....RW

This register is used for flow control.

7-0 Receive Buffer Count Available for Incoming Packet

Offset 99 - Flow Control 1 (CR1).....RW

7-6 Transmit Pause Frame Low Threshold
- 00 4 free Receive Buffer left
- 01 8 free Receive Buffer left
- 10 16 free Receive Buffer left
- 11 24 free Receive Buffer left**.....default**

5-4 Transmit XON Pause Frame High Threshold
- 00 24 free Rx Buffer left
- 01 32 free Receive Buffer left
- 10 48 free Receive Buffer left**.....default**
- 11 64 free Receive Buffer left

3 Xon/Xoff Mode in Flow Control
- 0 Disable .....default
- 1 Enable

2 Full Duplex Flow Control on Transmit Side
- 0 Disable .....default
- 1 Enable

1 Full Duplex Flow Control on Receive Side
- 0 Disable .....default
- 1 Enable

0 Half-Duplex Flow Control
- 0 Disable .....default
- 1 Enable

Offset 9B-9A - Pause Frame Timer .....RW

15-0 Pause_Timer Value in Outgoing Pause Frame

Offset 9D-9C - Software Timer 0.....RW

15-0 Software Timer with Single Shot

Offset 9F-9E - Software Timer 1 .....RW

15-0 Software Timer with Periodic Shot

WOL Configuration and Control

Offset A0 / A4 – Wake-On-LAN Set / Clear ..... RW

7 Wake Up Event Detect Network Status Change from Link On to Link Off
- 0 Disable..... default
- 1 Enable

6 Wake Up Event Detect Network Status Change from Link Off to Link On
- 0 Disable..... default
- 1 Enable

5 Wake Up Event Detect Magic Packet
- 0 Disable..... default
- 1 Enable

4 Wake Up Event Detect Unicast Packet
- 0 Disable..... default
- 1 Enable

3 Wake Up Event Detect Pattern 3
- 0 Disable..... default
- 1 Enable

2 Wake Up Event Detect Pattern 2
- 0 Disable..... default
- 1 Enable

1 Wake Up Event Detect Pattern 1
- 0 Disable..... default
- 1 Enable

0 Wake Up Event Detect Pattern 0
- 0 Disable..... default
- 1 Enable

Offset A1 / A5 - Power Configuration Set / Clear (PWCFG SET / CLR) ..... RW

7 PHY Power Down Option ..... default = 0
6 Internal Sticky Logic Control ..... always write 0
5 WOL Pin Signaling Control
- 0 Pulse.
- 1 Button ..... default

4 Legacy Wake On LAN
3 PCI_CFG_PME_SR Shadow
2 PCI_CFG_PME_EN Shadow
1 Legacy WOL_SR Shadow
0 Legacy WOL_EN Shadow

Offset A2 / A6 Wake On LAN Set/Clear..... RW

7-4 Reserved.....always reads 0
3 LED off enable
- 0 Disable..... default
- 1 Enable

2 Reserved
1 Wake-Up Event: Detect Pattern 4
- 0 Disable..... default
- 1 Enable

0 Wake-Up Event: Detect Pattern 5
- 0 Disable..... default
- 1 Enable

Offset A3 / A7 – WOL Configuration Set / Clear .....RW

7 Power Management Over .....PME_OVR
Forces Power Management Event Enable (PME_EN) for Legacy Use
0 Disable .....default
1 Enable

6 Shadow Full Duplex Control in Suspend Wake On LAN Logic
0 Disable .....default
1 Enable

5 Shadow Accept Multicast Address Control in Suspend Wake On LAN Logic
0 Disable .....default
1 Enable

4 Shadow Accept Broadcast Address Control In Suspend Wake On LAN Logic
0 Disable .....default
1 Enable

3 Reserved (Do Not Program) ..... default = 0

2 Reserved .....always writes 0

1 Reserved (Do Not Program) ..... default = 0

0 Reserved .....always writes 0

Offset A8 / AC – Wake-On-LAN Status 0 .....RWC

7 Wake Up Event Status of Network Status Change from Link On to Link Off

6 Wake Up Event Status of Network Status Change from Link Off to Link On

5 Wake Up Event Status of Magic Packet Filter

4 Wake Up Event Status of Unicast Packet Filter

3 Wake Up Event Status of Patten 3 Filter

2 Wake Up Event Status of Patten 2 Filter

1 Wake Up Event Status of Patten 1 Filter

0 Wake Up Event Status of Patten 0 Filter

Offset BF-B0 - WOL Pattern match CRC Data.....RW

Offset CF-C0 - WOL Pattern Match Byte Mask 0 .....RW

Offset DF-D0 - WOL Pattern Match Byte Mask 1 .....RW

Offset EF-E0 - WOL Pattern Match Byte Mask 2.....RW

Offset FF-F0 - WOL Pattern Match Byte Mask 3 .....RW

PHY Registers (00-1Fh)

Offset 0 - MI Control (3100h)..... RW

15 PHY Reset .....default = 0
(Software Control)

14 Loopback Mode
0 Disable..... default
1 Enable

13 Speed Select LSB
0 10
1 100 ..... **default**

12 Auto-Negotiation Process
0 Disable
1 Enable..... **default**

11 Power Down
0 Disable..... default
1 Enable

10 Electrically Isolate PHY from MII
0 Disable..... default
1 Enable

9 Auto-Negotiation Restart .....default = 0
(Software Control)

8 Duplex Mode Select
0 Half
1 Full ..... **default**

7 COL Test
0 Disable..... default
1 Enable

6-0 Reserved .....always reads 0

Offset 1 – Management Information Status (7849h)..... RO

15 Capable of 100 Base-T4 Operation.....def=0

14 Capable of 100 Base-TX Full Duplex .....**def=1**

13 Capable of 100 Base-TX Half Duplex .....**def=1**

12 Capable of 10 Base-TX Full Duplex .....**def=1**

10-7 Reserved .....always reads 0

6 Capable of Accepting MI Frames with MI Preamble Suppressed.....**def=1**

5 Auto-Negotiation Process Completed.....def=0

4 Remote Fault Condition Detected.....def=0

3 Capable of Auto-Negotiation Operation .....**def=1**

2 Link Status .....def=0

1 Jabber Condition Detected.....def=0

0 Capable of Extended Register.....**def=1**

Offset 2 – PHY Identifier 0 (0101h)..... RO

15-0 Company ID MSBs .....always reads 0101h

Offset 3 – PHY Identifier 1 (8F43h)..... RO

15-10 Company ID LSBs .....always reads 8Fh

9-4 Manufacturer's Part number .....always reads 43h

3-0 Manufacturer's Revision Number....always reads 0

Offset 4 (04h) – AutoNegotiation Advertisement Base Page (05E1h) ..... RW

15	**Next Page**	default = 0
14	**Acknowledge**	**RO**, default = 0
13	**Remote Fault**	default = 0
12-11	**Reserved**	always reads 0
10	**Flow Control**	**default = 1**
9	**100 Base-T4 Capable**	default = 0
8	**100 Base-TX Full DuplexCapable**	**default = 1**
7	**100 Base-TX Half Duplex Capable**	**default = 1**
6	**10 Base-TX Full Duplex Capable**	**default = 1**
5	**10 Base-TX Half Duplex Capable**	**default = 1**
4-0	**Protocol Select**	**default = 00001b**

Offset 5 (05h) –Auto Negotiation Link Partner Base Page Ability (0000h) ..... RO

15	**Next Page Indication**	default = 0
14	**Acknowledge**	default = 0
13	**Remote Fault**	default = 0
12-10	**Reserved**	always reads 0
9	**100 Base-T4 Capable**	default = 0
8	**100 Base-TX Full DuplexCapable**	default = 0
7	**100 Base-TX Half Duplex Capable**	default = 0
6	**10 Base-TX Full Duplex Capable**	default = 0
5	**10 Base-TX Half Duplex Capable**	default = 0
4-0	**Protocol Select**	default = 0

Offset 6 (06h) – Auto-Negotiation Expansion (0004h) .... RO

15-5	**Reserved**	always reads 0
4	**Parallel Fault Detect in Auto-Negotiation Process**	default = 0
3	**Link Partner Capable of Next Page Process**	def=0
2	**Capable of Next Page Process**	default = 0
1	**Page Received in Auto-Negotiation Process**	default = 0
0	**Link Partner Capable of Auto-Negotiation Process**	default = 0

Offset 7 (07h) – AutoNegotiation Advertisement Next Page (2001h) ..... RW

15	**Next Page**	default = 0
14	**Reserved**	always reads 0
13	**Message Page**	**default = 1**
12	**Acknowledge**	default = 0
11	**Toggle Bit**	RO, default = 0
10-0	**Message Code Field or Unformatted Code Field**	**default = 001h**

Offset 8 (08h) – Link Partner Advertisement Next Page (0000h) ..... RO

15	**Next Page**	default = 0
14	**Received Code Word Recognized**	default = 0
13	**Message Page**	default = 0
12	**Capable of Complying with Message**	default = 0
11	**Toggle Bit**	default = 0
10-0	**Message Code Field or Unformatted Code Field**	default = 0

Offset 10h – PHY Configuration 1 (0800h) ..... RW

15-11	**PHY Address**	**RO**
10	**Fiber Mode**	
	0 Disable	default
	1 Enable	
9	**SIP Mode Select**	**RO**
	0 Disable	default
	1 Enable	
8	**Force Link**	**RO**
	0 Disable	default
	1 Enable	
7	**Base 10 Low Squelch Level Select**	**RO**
	0 Disable	default
	1 Enable	

6-5 **Programmable LED Output Select**

	LED0	LED1	LED2	LED3
00	Link/Act	Speed	Duplex	COL.... def
01	Pwr/TxAct	Link/RxAct	Speed	Duplex
10	Speed100	Speed10	Act	Duplex
11	Pwr/TxAct	Link/RxAct	Speed	COL

4	**Repeater Mode**	**RO**
3	**PHYINT Output Select**	
	0 PHYINT	default
	1 MDIO	
2	**Symbol Mode**	
	0 Disable	default
	1 Enable	
1	**Reserved**	always reads 0
0	**nWay Force Mode**	RW, default = 0

Offset 11h - PHY Configuration 2 (F7FFh) .....

15	**Jabber Detect**	
	0 Disable	
	1 Enable	**default**
14	**Signal Quality Error Detect**	
	0 Disable	
	1 Enable	**default**
13	**Auto-Polarity Enable**	
	0 Disable	
	1 Enable	**default**
12	**Far End Fault Enable**	
	0 Disable	
	1 Enable	**default**
11	**Change Seed of Scrambler**	**Self Clearing**
	0 Disable	default
	1 Enable	
10-0	**New Seed**	default = 7FFh

Offset 12h – PHY Configuration 3 (0800h) .....RW

15 Bypass Scrambler and Descrambler Functions
- 0 Disable .....default
- 1 Enable

14 Bypass 4B5B Encoding and Decoding Functions
- 0 Disable .....default
- 1 Enable

13 Bypass Symbol Alignment Function
- 0 Disable .....default
- 1 Enable

12 Bypass NRZI Encoding and Decoding Functions
- 0 Disable .....default
- 1 Enable

11 Loss Sync Function..... Self Clearing
- 0 Disable
- 1 Enable **.....default**

10 Lost Sync Timer Select
- 0 722 usec .....default
- 1 2 msec

9-0 Reserved ..... always reads 0

Offset 13h – PHY Interrupt Mask (FFFCh) ..... RW

15 Mask Interrupt Function
- 0 Disable
- 1 Enable**..... default**

14 Mask Interrupt on Link-Up Status
- 0 Disable
- 1 Enable**..... default**

13 Mask Interrupt on Link-Fail Status
- 0 Disable
- 1 Enable**..... default**

12 Mask Interrupt on Link Status Change
- 0 Disable
- 1 Enable**..... default**

11 Mask Interrupt on Auto-Negotiation Process Complete
- 0 Disable
- 1 Enable**..... default**

10 Mask Interrupt on Page Received in Auto-Negotiation Process
- 0 Disable
- 1 Enable**..... default**

9 Mask Interrupt on Jabber Condition Detect
- 0 Disable
- 1 Enable**..... default**

8 Mask Interrupt on Invalid Symbol Received
- 0 Disable
- 1 Enable**..... default**

7 Mask Interrupt on SSD Delimiter Error Detected
- 0 Disable
- 1 Enable**..... default**

6 Mask Interrupt on ESD Delimiter Error Detected
- 0 Disable
- 1 Enable**..... default**

5 Mask Interrupt on Signal Quality Error Detected
- 0 Disable
- 1 Enable**..... default**

4-2 Reserved (Do Not Program).....default = 111b

1-0 Reserved .....always reads 0

Offset 14h – PHY Status (0000h).....RO

15 **Polarity Inversion Base10-Tx**
- 0 Disable .....default
- 1 Enable

14 **Link Up Status** ..... default = 0
13 **Link Fail Status**..... default = 0
12 **Link Status** ..... default = 0
11 **Auto-Negotiation Process Complete** ..... default = 0
10 **Page Received in Auto-Negotiation Process**.....
..... default = 0
9 **Jabber Condition Detect** ..... default = 0
8 **Error Code Symbol Received** ..... default = 0
7 **Start of Stream Delimiter Error**..... default = 0
6 **End of Stream Delimiter Error** ..... default = 0
5 **Signal Quality Error Detected**..... default = 0
4-2 **Reserved (Test Status)**..... default = 000b
1 **PHY Speed Status**..... default = 0
0 **PHY Duplex Status**..... default = 0

Offset 19h – Power Control.....RW

15-8 **Reserved** ..... always reads 0
7 **Power Saving Status**
- 0 Low Power Enable.....default
- 1 Force Power Saving Mode

6-0 **Reserved** ..... always reads 0

FUNCTIONAL DESCRIPTIONS

The VT6105M PCI bus master 10/100 Mbps fast Ethernet controller is a CMOS VLSI chip designed for easy implementation in CSMA / CD IEEE 802.3u 10/100 Mbps Ethernet networks. Significant features include: twisted-pair wiring interface, Plug and Play compatibility, 32-bit bus mastering, powerful buffer management and receive and transmit functions for early interrupt transmit and receive.

The VT6105M integrates the entire bus interface of PCI systems, complying with PCI Specification v2.1 and v2.2. The VT6105M supports the on-chip 100Base-TX / FX layer transceiver.

Host Bus Interface Control Logic

PCI Master Function

The VT6105M supports a descriptor-based communication list between hardware and software on both transmitting and receiving signals. The DMA scheduler fetches the transmit and receive descriptors via PCI bus mastering to check if free buffers are available to store receive packets and scheduled transmission requests.

Data transfer between the system buffers and internal FIFOs in the VT6105M are executed by the internal PCI DMA controller using a bus mastering linear bursting scheme. An advanced internal bus arbitration scheme is imlemented to improve bus utilization and service priorities.

The VT6105M also supports a Look Ahead Scheduler which queues multiple transmit frames and back-to-back service receive packets.

When receive or transmit processes are complete, the VT6105M writes back the transfer and network status to the indexed descriptors to release descriptor ownership.

PCI Slave Function

VT6105M supports PCI slave-register I/O and memory-mapped I/O cycles for command and status registers, PCI configuration cycles for Plug & Play BIOS and memory-read cycles for Boot ROM code shadowing.

Buffer Management

The VT6105M hardware controller and drivers communicate through two data structures:

1. Control and status register (CSR)
2. Descriptor entries and data buffers

During initialization, the drivers create the structure of the Transmit and Receive descriptors in physical memory and decide the base address for the Receive and Transmit descriptor rings, which are written to registers CSR6 (Current Receive Descriptor Address) and CSR7 (Current Transmit Descriptor Address) respectively. The number of entries contained in the descriptor rings and the buffers reserved in physical memory for Receive and Transmit descriptors are set up during initialization.

Each of the descriptor entries must occupy a contiguous area of memory. The Receive (Transmit) Descriptor DMA register of the CSR also keeps the content of the current and next Receive and Transmit Descriptor.

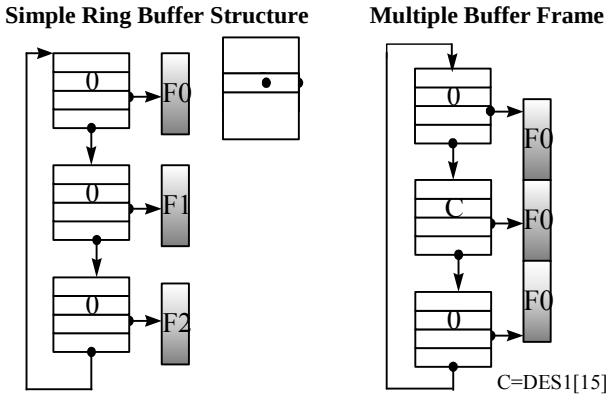


Figure 3. Buffer Structure

For Reception, when the data packets in the receive FIFO are transferred to system memory, the controller will proceed to write back the current packet reception status to the receive descriptor and then update the transmit interrupt status in the ISR.

When transmitting data, the controller starts the DMA cycle and brings the data from memory to the Tx FIFO register and updates the status information of the Transmission Descriptor DMA Register after transmission is complete. The controller then proceeds to write back to the descriptor in memory using another DMA cycle.

Receive Descriptor Packet Layout (RD)

The Receive Descriptor packet layout provides a data buffer address, byte-count, and a next descriptor address. The chain bit allows data storage to span multiple data buffers and is compatible with various types of memory-management schemes.

	31	30-16	0-15
RDES0	0	Rx Length Field	RSR
RDES1	IPKT	PQSTS	Rx_Buffer_Size
RDES2	Rx_Buffer_Start_Address		00
RDES3	Next_Rx_Desc_Address		

Figure 4. Receive Descriptor Packet Layout

The Receive Descriptor Layout consists of four levels of data: RDES0, RDES1, RDES2, and RDES3.

Table 4. Receive Descriptor 0 (RDES0)

Bit		Symbol	Description
31		OWN	**Owner.** This bit is controlled by the driver, which enables the bit when initialized. 1 indicates that a descriptor is free for the VT6105M to use. 0 means this descriptor is being used by the VT6105M.
30-27		-	-reserved-
26-16		Rx_Length [10-0]	**Receive Length**
15-8			**Receive Status Register**
	15	RXOK	**No Receive Errors**
	14	VIDHIT	**Receive Tagged Packet with VLAN ID Hit**
	13	MAR	**Accept Multicast Address Packets**
	12	BAR	**Accept Broadcast Address Packets**
	11	PHY	**Accept Physical Address Packets**
	10	CHN	**Chain Buffer** - Always = "1"
	9	STP	**Packet Start** - This occurs in the Descriptor ring structure: STP=1 EDP=1 - Single buffer; STP=1 EDP=0 - Another buffer chained; STP=0 EDP=1: Packet end indication; STP=0 EDP=0 – invalid setting
	8	EDP	**Packet End Indication**
	7	BUFF	**Descriptor Link Structure Error**
	6	FRAG	**Packet was a Fragment**
	5	RUNT	**Runt Package Received**: length < 64 bytes
	4	LONG	**Long Package Received**: length > 1518 bytes
	3	FOV	**FIFO Overflow**
	2	FAE	**Frame Align Error**
	1	CRCE	**CRC Error**: receive frame checksum error
	0	RERR	**Receive Error**: RERR = CRCE | FAE | FOV | BUFF | SERR

Table 5. Receive Descriptor 1 (RDES1)

Bit	Symbol	Description
31-24	IPKT	**Interesting Packet.** Address defined in Multicast-CAM address register
23-16	**PQ Status**	
23	RXLERR	**Receive Length Check Error**
22	SNAPTAG	**Snap Packet with 802.1q Compliant Tag**
21	IPOK	**IP Checksum Validation OK**
20	TUOK	**TCP / UDP Checksum Validation OK**
19	IPKT	**Receive an IP Packet**
18	TCPKT	**Receive a TCP Packet**
17	UDPKT	**Receive a UDP Packet**
16	TAG	**Receive a Tagged Packet**
15	R	
14-11	-	-reserved-
10-0	Rx_Buffer_ Size	**Receive Buffer Size**

Table 6. Receive Descriptor 2 (RDES2)

Bit	Symbol	Description
31-2	Rx_Buffer_ Start_Addr	**Register Buffer Start Address** Double word alignment (bits 1:0 always 00b)

Table 7. Receive Descriptor 3 (RDES3)

Bit	Symbol	Description
31-2	Next_Rx_ Desc_Addr	**RD Branch Address.** Next linked receive descriptor address

Transmit Descriptor Packet Layout (TD)

The Transmit Descriptor packet layout provides a data buffer address, byte-count, and a next descriptor address. The chain bit allows data storage to span multiple data buffers and is compatible with various types of memory-management schemes.

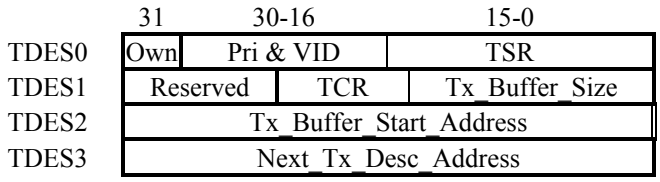


Figure 5. Transmit Descriptor Packet Layout

The Transmit Descriptor Layout consists of four levels of data: TDES0, TDES1, TDES2, and TDES3.

Table 8. Transmit Descriptor 0 (TDES0)

Bit	Symbol	Description
31	OWN	**Owner**. This bit is controlled by the driver. 1 indicates that a Transmit request is scheduled. 0 means this descriptor is used by VT6105M. The driver must enable this bit when initialized.
30-28	PRI	**Priority Tag.** 802.1p priority bits
27-16	VID	**VLAN ID.** 802.1q Virtual LAN Identifier
15-0	TSR	**Transmit Status Register**
15	TERR	**Transmit Error** 0: Tx successfully 1: ABT|UDF (for definitions see entries in this table)
14-12	-reserved-	**-reserved-**
11	UDF	**FIFO Underflow**
10	CRS	**Carrier Sense Lost Detect**
9	OWC	**Out of Window Collision**
8	ABT	**Excessive collision Tx abort**
7	CDH	**CD Heartbeat Check Failure** (valid in 10Base-T mode)
6-5	-reserved-	**-reserved-**
4	COLS	**Collision Detect**
3-0	NCR	**Number of Collision Retries**

Table 9. Transmit Descriptor 1 (TDES1)

Bit		Symbol	Description
31-24		-reserved-	**Reserved.**
23-16		TSR	**Transmit Control Register**
	23	IC	**Interrupt Control** 0: No interrupt when Transmit OK 1: Interrupt when Transmit OK
	22	EDP	**End of Transmit Packet**
	21	STP	**Start of Transmit Packet**, in Descriptor ring structure STP=1 EDP=1 - single buffer per packet STP=1 EDP=0 - packet segment STP=0 EDP=1 - packet end indication STP=0 EDP=0 - invalid setting
	20	TCPCK	**Request TCP Checksum Calculation**
	19	UDPCK	**Request UDP Checksum Calculation**
	18	IPCK	**Request IP Checksum Calculation**
	17	TAG	**Insert Tag Request**
	16	CRC	**Disable CRC Generation**
15		CHN	**Chain Structure** 1 Indicates a chain structure 0 indicates a ring structure.
14-11		-reserved-	Always reads 0
10-0		Tx_Buffer_ Size	**Transmit Buffer Size** Always reads 0

Table 10. Transmit Descriptor 2 (TDES2)

Bit	Symbol	Description
31-0	Tx_Buffer_ start_address [31:0]	**Transmit Buffer Start Address** Byte-oriented transmit data buffer starting address

Table 11. Transmit Descriptor 3 (TDES3)

Bit	Symbol	Description
31-4	Next_Tx_ Desc_Address [31:4]	**TD Branch Address.** Next linked transmit descriptor start address
3-1	TDCTL[3-1]	**Reserved**
0	TDCTL[0]	**Interrupt Control.** 0 = issue interrupt for this packet 1 = no interrupt generated

FIFO and Control Logic

The VT6105M incorporates two independent deep memory FIFOs for data that is transmitted and received between the system interface and the network interface. The FIFOs provide temporary data storage and free the host system from the real-time demands of the network.

The VT6105M implements enhanced receive FIFO management logic to handle multiple received data packets that are transferred to the system data buffer. This ability can reduce packet loss due to PCI bus mastering arbitration latency. The PCI bus mastering arbitration latency is the time from a request issued by the master to when the receiver (arbiter) performs the request.

Network Interface

The VT6105M controller supports 100Base-TX and 100Base-FX transceivers, and provides an independent 10 / 100 BaseT transceiver interface to an external 1:1 magnetic transceiver.

Auto-Negotiated 10Base-T / 100Base-T / Fiber Support

The 802.3u Auto-Negotiation specification defines the automatic negotiation of signaling rate and duplex mode between two ends of a twisted pair link segment. The VT6105M is integrated with a 802.3u-compliant Auto-Negotiation Mechanism for 10Base-T and 100Base-TX medium types.

The VT6105M supports media port selection in three ways that depend on the state of the internal configuration:

- A specific, predetermined port
- An auto-negotiated port
- Force 100 Fx Fiber mode by system configuration

Through Auto-Negotiation, the VT6105M attempts to negotiate a 10Base-T or 100Base_TX link with a remote adapter. Immediately after power up, the VT6105M starts the Auto-Negotiation process by advertising the capabilities and listening for indication of the link partner's capabilities. After the Auto-Negotiation process is complete, the VT6105M can determine if a link is established or not as well as the speed and duplex type of the connection.

100BaseT Transceiver Auto MDI/MDIX Configuration

The VT6105M supports MDI / MDIX functions for user-friendly installation of switch hubs, peer-to-peer PCs, cable modems, and ADSL modems with crossover TP usage.

LED Status and PHY Force Fiber Mode Strapping

VT6105M network status information is available on four LED output pins. The LEDs reflect network status per the "LED Select" bits in PHY register Rx10[6:5] and can be set up to indicate various status functions such as the transmit, receive and collision activities, link status, and link polarity. LED Function Definition is summarized in Table 12 below.

Table 12. LED Status

LEDSEL	LED0 (Blinking)	LED1	LED2	LED3
00	Link / Active	Speed	Duplex	COL
01	Power / TxAct	Link / RxAct	Speed	Duplex
10	Spd100	Spd10	Active	Duplex
11	Power / TxAct	Link / RxAct	Speed	COL

Content-Addressable-Memory-(CAM)-Based Perfect filtering

The VT6105M enhanced address recognition logic function uses Content Addressable Memory (CAM) technology to support multicast, interesting-packet perfect-filtering, and VID perfect-filtering for Virtual LAN (VLAN) support:

Programming CAM

The VT6105M driver initializes the CAM through the following algorithm:

```
enable CAM controller, CAMEN = 1
set Active CAM, (VCAMSL)
set CAM entry address, (CAMADD)
set CAM entry data. ( M_CAM : 0x10 ~ 0x15)
        (V_CAM : 0x16 ~ 0x17)
set CAMWR.
wait 1us before next CAMWR
```

Reading CAM

The VT6105M driver downloads the CAM contents through the following algorithm:

```
enable CAM controller, CAMEN = 1;
set Active CAM, (VCAMSL)
set CAM entry address (CAMADD)
set CAMRD.
Wait 2us
read CAM content from data port
(M_CAM : 0x10 ~ 0x15)
(V_CAM: 0x16 ~ 0x17)
```

Multicast Perfect-Filtering

Multicast perfect filtering uses the following steps.

- Program Multicast Address CAM (MCAM) with accepted multicast address.
- Turn on the CAMMASK bits to enable related Multicast Address CAM entries.
- Turn on AM, and incoming multicast packets will be filtered with perfect address.

If the number of multicast addresses are larger than 32, the multicast hash tables can also be used.

CAM content does not clear after a rest action. CAMMASK can only be controlled to handle the active entries.

Interesting-Packet Perfect-Filtering

Interesting packets are a group of packets with a specified Multicast Address. The VT6105M provides circuitry that can filter a maximum of 8 interesting packets. The hits of 8 former M_CAM entries are stored and written-back to the RD status.

The following two operations can be performed by the VT6105M:

- Programming the interesting packet address into M_CAM.
- For each incoming packet, check the RD.IPKT field to see which interesting packet was received.

Checksum Offload

The VT6015M provides automatic TCP/IP checksum insertion and verification. On Transmission, the Host requests TCP/IP checksum offloading by setting the control bit in the transmit descriptor header control field. A packet request for checksum offload will change the transmit scheduling from Threshold mode to Store-and-Forward mode, causing some latency of the packet transmission.

On reception, when the checksum offload enable bit is set, every packet is filtered for the presence of IP, TCP, and UDP headers. For any headers that are found, the checksum logic will calculate and compare the headers with the related fields in the packet. Mismatches are flagged as a checksum error and the status is kept in the write back status field and transferred to the host by the normal packet reception write back flow.

For the VT6105M to perform checksum offload, the following requirements must be met:

- Packets can only work in IPv4 networks only. Packets of other IP versions will be ignored
- IP forms are EtherType = 0800h, IEEE 802.2 and SNAP.
- Fragmented IP datagrams are not supported.
- VLANs must be IEEE 802.1q compliant

VLAN

The VT6105M supports the IEEE 802.1q Virtual Local Area Network (VLAN). In a VLAN environment, the controller will respond to a range of individual addresses that allow multiple VLAN support.

IEEE 802.1q VLANs

802.1q frames have 4 extra bytes over normal 802.3 frame formats. Two of the bytes contain a special type (TPID) and the other two bytes contain a 12-bit VLAN ID number, 3 bits of priority and a "token Ring encapsulation" bit. The VT6105M will accept an oversized frame on a 802.1q packet if it is greater than MaxPktSize+4.

With frame tagging, each VT6105M can support up to **32** IP address assignments on a single network connection. This allows servers to be accessed from systems within multiple IP subnets without passing through routers. It also allows users to define multiple application VLANs to partition traffic for performance and security purposes.

The VT6105M supports the following Multiple Virtual LAN (VLAN) requirements:

- Long frame support (1518 + 4) bytes
- VLAN tag insertion for transmit packets
- VLAN tag detection and removal for receive packets
- VLAN status could be written back to the Receive Descriptor

IEEE 802.1p Priority Transmit

To meet the demands of current multimedia applications and maintain Quality Of Service (QoS), the VT6105M supports IEEE 802.1p and provides eight levels of priorities. The priority DMA scheduler maintains a flexible queuing usage depending on the driver's setting. The VT6105M hardware and software maintain 8 TD queues in the advanced priority DMA scheduler and also provide a non-blocking mode for high performance.

Flow Control

The VT6105M supports half duplex Jam-based and IEEE802.3x flow control schemes while in full duplex.

When the VT6105M detects that the system is busy it receives buffers or a signal to indicate that the internal FIFOs are filling up.

In half duplex mode, the MAC will send a jam pattern automatically when the addressed packets come to stop the transmission from the source station. In full duplex mode, the VT6105M will generate a PAUSE control frame to inform the source station of the stopping of transmission for a specified period of time defined in the PAUSE frame. After the busy condition is cleared, the VT6105M will send another PAUSE control frame with pause_time (0000h) to inform the source station to prepare to receive packets.

The VT6105M also implements detection logic to filter the incoming pause control frame. When a valid PAUSE control frame is detected, the VT6105M will enter the backoff state after the current transmission completed and wait for the specified period of time defined in the received PAUSE frame operation. The VT6105M will re-transmit other packets in the transmit queue after receiving a new pause frame with pause_time of 0000h or when the pause timer is expired. Also, the IEEE802.3x flow control capability is the negotiated results from N-way and can be optionally disabled.

Statistics

The VT6105M provides network traffic statistics to ease network management:

Network Error	Description
No Rx Buffer Space	This specifies the number of frames that the NIC cannot receive due to lack of NIC receive buffer space. Some NICs do not provide the exact number of missed frames; they provide only the number of times at least one frame is missed.
Rx Error Packets	Packets received with errors. This counter is incremented for each packet received with errors. The count includes packets that are automatically rejected from the FIFO due to both wire errors and FIFO overruns.
Rx Frame Check Sequence Errors	Packets received with frame check sequence errors. This counter is incremented for each packet received with a Frame Check Sequence error (bad CRC). **Note:** For the MII interface, an FCS error is defined as a resulting invalid CRC after CRS goes invalid, and an even number of bytes have been received.
Rx Missed Packet Errors	Packets missed due to FIFO overruns. This counter is incremented for each reception aborted due to data or status FIFO overruns (insufficient buffer space).
Rx Frame Alignment Errors	Packets received with frame alignment errors. This counter is incremented for each packet received with a Frame Check Sequence error (bad CRC). **Note:** For the MII interface, an FAE error is defined as a resulting invalid CRC on the last full octet, and an odd number of nibbles have been received (Dribble nibble condition with a bad CRC).
Rx Frame Too Long	Packets received with length greater than 1518 bytes (packet too long). This counter is incremented for each packet received with greater than the 802.3 standard maximum length of 1518 bytes.
Rx In-Range-Length Errors	Packets received with In Range Length errors. This counter increments packets received with a MAC length / type value between 64 and 1518 bytes inclusive, that does not match the number of bytes received. This counter also increments for packets with a MAC length / type field of less than 64 bytes and more than 64 bytes received.
Rx Bad Opcodes	Packets received with a valid MAC control type and an opcode for a function that is not supported by the device.
Rx Pause Frames	MAC control Pause frames received.
Tx Pause Frames	MAC control Pause frames transmitted.
Tx SQE Errors	Loss of collision heartbeat during transmission. This counter is incremented when the collision heartbeat pulse is not detected by the PMD after a transmission.
Rx Symbol Errors	Packets received with one or more symbol errors. This counter is incremented for each packet received with one or more symbol errors detected. **Note:** For the MII interface, a symbol error is indicated by the RXER signal becoming active for one or more clocks while the RXDV signal is active (during valid data reception).

MIB Read Access

The following action takes place in MIB read access.

- After HardReset / SoftReset, all MIB counters are reset to zero
- Turn on MIBCR.MIBEN.
- Select MIB indication threshold via MIBCR.MIBHALF.
- As CNTI occurs, read all MIB counters by 12 continuous IOR (MEMR) MIBPORT.
- All MIB counters will be auto-cleared.
- After all MIB counters have been read, clear ISR
- If any uncertain event, break the MIB collection routine (12 continuous read), MIBCR.MIBRTN can be used to reset the MIB read pointer to zero.

EEPROM Interface

EEPROM Direct Programming

The VT6105M features an easy way to program the external serial EEPROM directly. Setting EELOAD (Rx78[7]) and DPM (Rx74[4]) make the VT6105M enter Direct Programming Mode. In this mode the user can directly control the EEPROM interface signals by writing to the EECSR register (Rx74). EECS (bit 3), EESK (bit 2), and EEDI (bit 1) will be driven onto the EECS, EESK, and EEDI pins respectively. These outputs will be latched so the user can generate the EEPROM interface signals per the 93C46 data sheet.

To read EEPROM data, the EEPROM interface must generate signals onto the EECS, EESK, and EEDI pins at the same time as data is read from the EEDO input via the EEDO bit (bit 0). Reading the EEDO bit during programming will not affect the latched data on the EECS, EESK, and EEDI outputs. When the EEPROM has been programmed and verified (including the lower byte of 0Fh with 73h), the VT6105M must be reset to return to normal operation and read in the new data.

Direct Programming Mode is mainly used for production to program every bit of the EEPROM. Once the lower byte of 0Fh has been programmed with 73h and a power-on reset has been performed, EEPR (Rx74[7]) will be set so the contents of the EEPROM may not be changed.

EEPROM Embedded Programming

If the upper byte of 0Fh of the serial EEPROM has been programmed to 73h when the VT6105M is loading the EEPROM data during power-on reset, the EEPR bit of Signature Register will be set to prohibit Direct Programming mode. However, configuration registers A, B, and C are programmed using Embedded Programming mode by following the routine specified in the example code below. This operation will work regardless of the value of EECONFIG. The setting of the EELOAD bit of Configuration Register B starts the EEPROM write process. Care should be taken not to accidentally modify the "polarity" (POL) and "good link" (GDLNK) bits because these two bits return the value indifferent from the setting. This programming process is ended when the EELOAD bit goes to zero.

```
EEPROM_EMB_PROG ( )
{     //    defined constant:
CONFIG_B,  EELOAD
//    declared register: value,
      config_for_A, config_for_B,
      config_for_C
//    declared function:
DISABLE_INTERRUPTS,
ENABLE_INTERRUPTS, READ, WRITE, WAIT
            DISABLE_INTERRUPTS ( );
            value = READ (CONFIG_B);
            value = value | EELOAD;
            WRITE (CONFIG_B, value);
            READ (CONFIG_B);
            WRITE (CONFIG_B,
config_for_A);
            WRITE (CONFIG_B,
config_for_B);
            WRITE (CONFIG_B,
config_for_C);
            while (value || EELOAD)
      {
            value = READ (CONFIG_B);
            WAIT ( );
      }
      ENABLE_INTERRUPTS ( );
```

EEPROM Contents

The VT6105M supports a 93C46 external Serial ROM, which may be used, when a BootROM is not used, to store the Ethernet ID, sub-vendor ID, and chip configurations (listed in Table 13 below):

Table 13. EEPROM Contents Chip Configurations

Offset ID	Chip Configuration	
	Bit [15:8]	Bit [7:0]
00h	Ethernet Global ID [15:8]	Ethernet Global ID [7:0]
01h	Ethernet Global ID [31:24]	Ethernet Global ID [23:16]
02h	Ethernet Global ID [47:40]	Ethernet Global ID [39:32]
03h	PHY ANAR	Reserved (always 00h)
04h	PCI Configuration Sub-System ID [15:0]	PCI Configuration Sub-System ID [7:0]
05h	PCI Configuration Sub-Vendor ID [15:0]	PCI Configuration Sub-Vendor ID [15:0]
06h	Device ID 1	Device ID 0
07h	Vendor ID 1	Vendor ID 0
08h	Data Select	PCI Power Management Capability Setting
09h	Auxiliary Current	PMU Data
0Ah	Reserved (always 00h)	Reserved (always 00h)
0Bh	PCI Configuration Maximum Latency	PCI Configuration Minimum Grant
0Ch	Bus Control 1	Bus Control 0
0Dh	Configuration B	Configuration A
0Eh	Configuration D	Configuration C
0Fh	EEPROM Checksum (default = 55h)	EEPROM Programmed Indicator (73h)

The "Power Management Capability Setting" byte includes the following:

- Bit-0: D0_En - D0 state capable
- Bit-1: D1_En - D1 state capable
- Bit-2: D2_En - D2 state capable
- Bit-3: D3h_En - D3 hot state capable
- Bit-4: D3c_En - D3 Aux power state capable
- Bit-5: D1_Dis - Disable D1 state support
- Bit-6: D2_Dis - Disable D2 state support
- Bit-7: DSI - DSI in PMU register

Interrupt Control

Data consists of an entire frame or part of a frame that is within the size of a single Ethernet frame. Buffers contain only data; all buffer status is maintained in the descriptor. Data chaining is enabled or disabled by the Chain bit in DES1[15]. Interrupt control may also be enabled or disabled by DES1[23].

Interrupt generation control for packet transmission and reception are defined in transmit and receive descriptors.

When the Interrupt Control bit (DES1[23]) is set to 1, the receive or transmit interrupt is generated regardless of whether the completed frame has been transmitted or received. This feature enables the Operating System to pre-fetch the frame header or save the interrupt service overload.

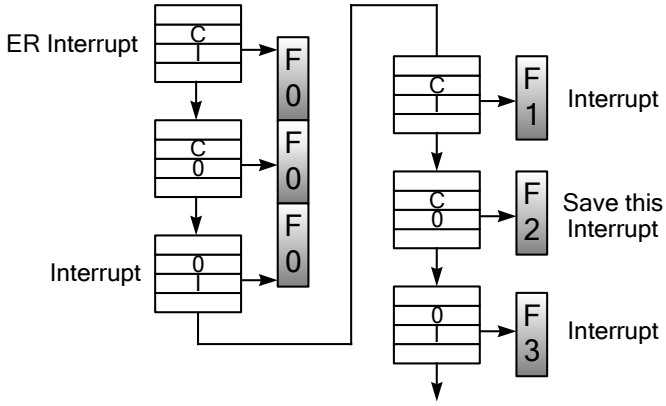


Figure 6. Interrupt Control

Flow Control

The VT6105M is Jam based in half-duplex and supports the IEEE 802.3x flow control scheme while in full duplex. This occurs when the VT6105M detects the receive buffers or when the external FIFO is running up.

In half duplex mode, the MAC sends jam patterns automatically when the addressed packets are stopping transmission from the source station. In full duplex mode, the VT6105M will generate a Pause control frame to inform the source station to stop transmission for a specified period of time defined in the Pause frame. After the busy condition is clear, the VT6105M will send another Pause control frame with pause_time (0000h) to inform the source station to prepare packet reception.

The VT6105M also implements detection logic to filter incoming pause control frames. When a valid Pause control frame is detected, the VT6105M enters the Backoff state after the current transmission is completed and waits for the specified period of time defined in the received Pause frame to operate. The VT6105M will retransmit other packets in the transmit queue after receiving a new pause frame with pause_time (-0000h) or when the pause timer has expired.

Also, IEEE 802.3x flow control capability results from N-Way auto-negotiation and can be optionally disabled.

Power Management

The VT6105M is compliant with ACPI V1.0, PCI Power Management V1.1 and Network device class power management V1.0a specifications. It meets PC97 / PC98 / PC99 / PC2001 and Net-PC requirements. VT6105M can wake up a system in power-down mode. Using four wake-up events, the VT6105M wakes up a system via the PME# signal and restores the system to its running state.

Wake-Up Events

- **Link Status Change**: If the link state is either connect or disconnect, PME# is generated when the link state changes
- **Magic Packet**: When the VT6105M is set to magic packet mode, it requires that a received packet qualify as a Magic Packet
- **Magic Packet Pattern**: The Magic packet pattern (six FFh bytes + 16 times Source Address duplication) matches the destination address of the received magic packets. The Magic register (RxA0[5]) is set to enabled and the VT6105M will receive the packet.
- **Unicast Physical Address Match**: When the VT6105M is set to Unicast mode, it requires a received packet to qualify as a unique individual address. The Unicast register bit (RxA0[5]) is set to enabled and the VT6105M will receive the packet.
- **MS-Defined Pattern Match**: When the stations shut down after an operating system is loaded, the IP address, station name or other defined values are set by the drivers to VT6105M
  - IP (ARP)
  - Name Query
  - NET BIOS
  - VIA defined

Table 14. Power States

Device State	Conditions	PCI mA	AUX mA	Action
D0	PCI = 33MHz, MAC = 25MHz, Tx, Rx Active	28	11	Full function
D1, D2	PCI = 33MHz, MAC = 25MHz, PCI bus transaction Idle	18	9	Wake up event detection
D3 hot	PCI Clock Idle, MAC = 25MHz, Tx off, Rx on	9	8	Wake up event detection
D3 cold	PCI power off, MAC = 25MHz, Tx off, Rx on	9	8	Wake up event detection

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 15. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comment
T_S	Storage Temperature	-55	125	° C	
T_C	Case Operation Temperature	0	110	° C	
Ta	Ambient Operation Temperature	0	70	° C	
Θjc	Thermal Resistance	20.6		° C/w	
V_{CC33}	3.3V I/O Supply Voltage	V_{CC33} - 0.3	V_{CC33} + 0.3	Volts	3.3 V
V_{CC25}	2.5V Core Voltage	V_{CC25} - 0.25	V_{CC25} + 0.25	Volts	2.5 V
V_{CCA}	2.5V Analog Voltage	V_{CCA} - 0.25	V_{CCA} + 0.25	Volts	2.5 V
V_{CCRAM}	2.5V Internal SRAM Voltage	V_{CCRAM}-0.25	V_{CCRAM} + 0.25	Volts	2.5 V
—	ESD Rating	—	2500	Volts	

Note: Stress above the conditions listed may cause permanent damage to the device Functional operation of this device should be restricted to the conditions described under operating conditions.

DC specifications

T_C = 0-110° C,V_{CC33} = 3.3V ±5%, V_{CC25} = V_{CCRAM} = V_{CCA} = 2.5V ±5%, GND=0V

Table 16. DC Specifications

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	–0.5	0.8	Volt	
V_{IH}	Input High Voltage	2.0	V_{CC33} + 0.3	Volt	
V_{OL}	Output Low Voltage	—	0.45	Volt	I_{OL} = +4.0 mA
V_{OH}	Output High Voltage	2.4	—	Volt	I_{OH} = –1.0 mA
I_{IL}	Input Leakage Current	—	±10	uA	0 < V_{IN} < V_{CC33}
I_{OZ}	Tristate Leakage Current	—	±20	uA	0.45 < V_{OUT} < V_{CC33}

Power Consumption

Table 17. VT6105M Power Consumption

Power Consumption (Whole Card / No Boot ROM)	**100Mbps**		**10Mbps**	
	Current (mA)	**Wattage (W)**	**Current (mA)**	**Wattage (W)**
D0 (Without Cable)	48	0.12	48	0.12
D0	118	0.29	151	0.37
D3 cold (Without Cable)	40	0.1	40	0.1
D3 cold	110	0.27	40	0.1
D3 cold (Power Down)	7	0.01	7	0.01

Timing Specifications

PCI Bus Master

Descriptor Fetch - Burst Read

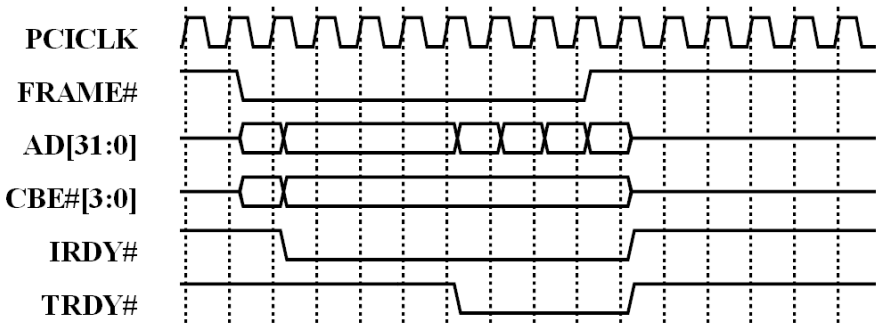


Figure 7. Descriptor Fetch

Status Write Back - Memory Write

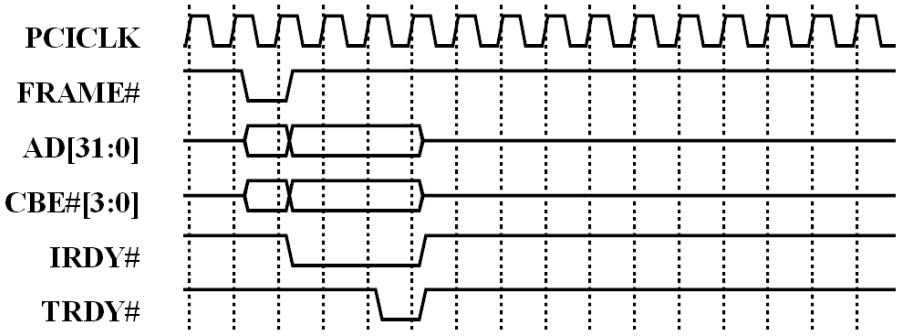


Figure 8. Write Back Status to Descriptor

Tx FIFO DMA - Burst Read with Memory-Read-Line, Memory-Read-Multiple-Enhance Commands

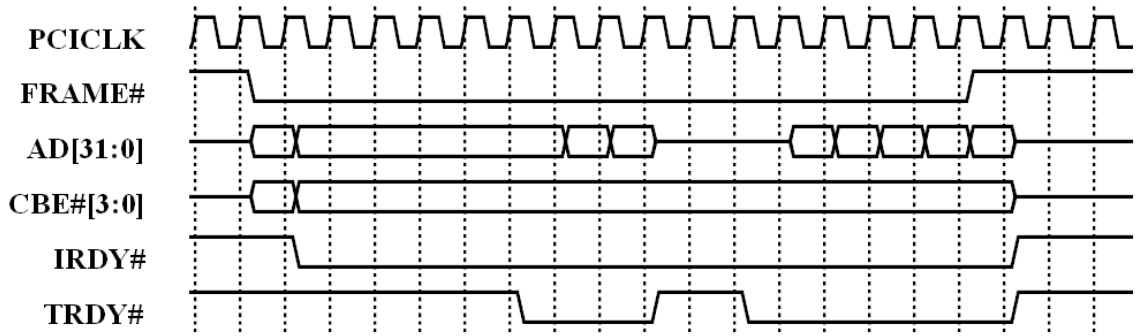


Figure 9. Memory Read (Tx FIFO DMA)

Rx FIFO DMA - Burst Memory Write

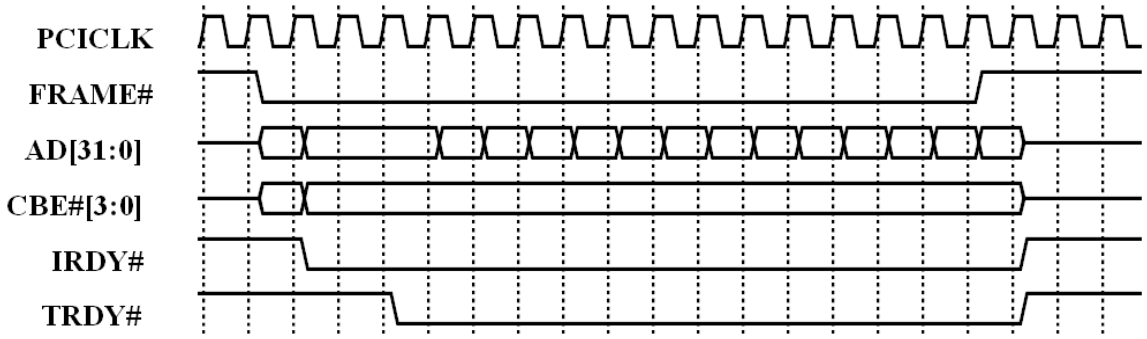


Figure 10. Memory Write (Rx FIFO DMA)

PCI Bus Slave

I/O Read / Write

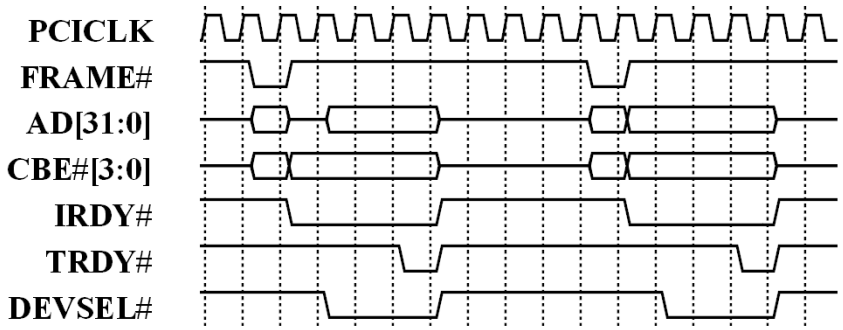


Figure 11. I/O Read / Write

Configuration Read / Write

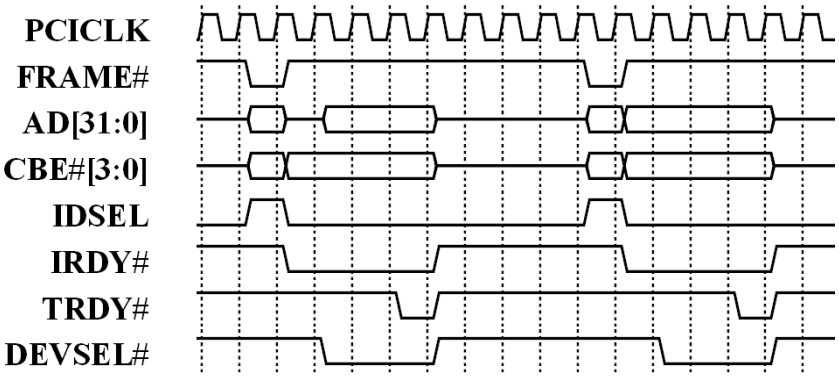


Figure 12. Configuration Read / Write

BootROM

Boot ROM Access Timing (with PCI Delay Transaction)

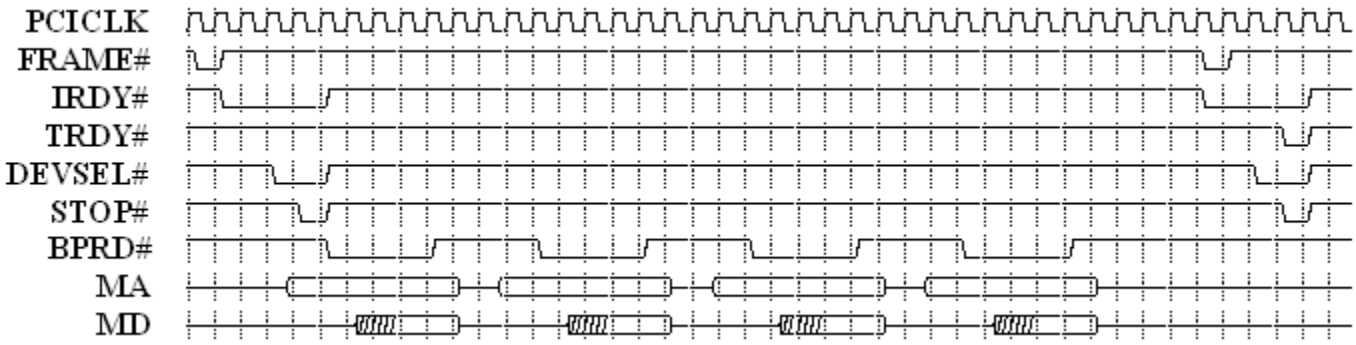


Figure 13. Boot ROM Access (with Delay Transaction)

BootROM Access Timing (without Delay Transaction)

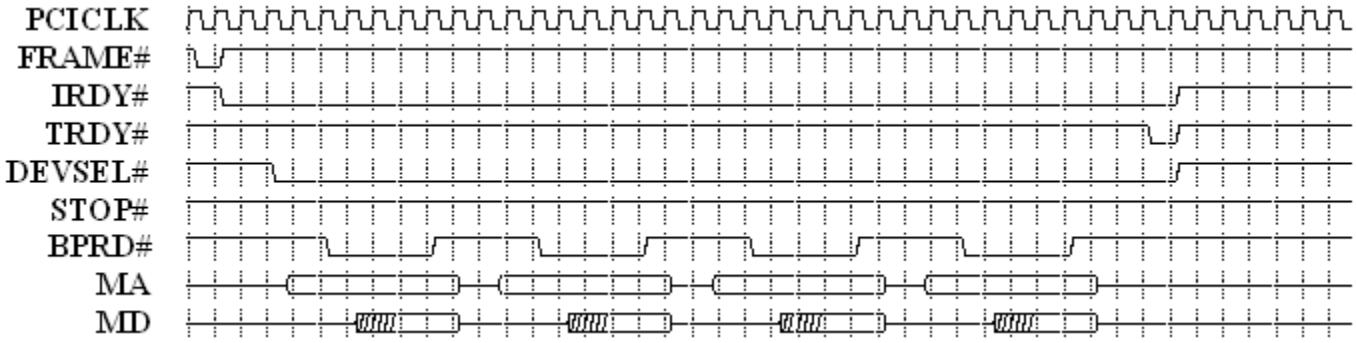


Figure 14. Boot ROM Access Timing (without Delay Transaction)

Embedded Flash Cycle Timing

Flash Write Timing (WE# Controlled Only)

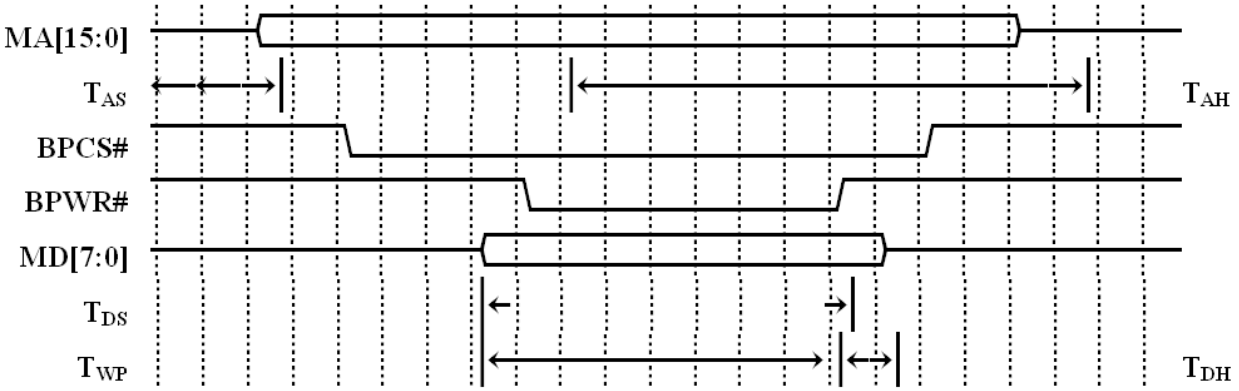


Figure 15. Flash Write Timing (WE# Controlled Only)

Symbol	Parameter	Min	Typ	Max	Unit
T_{AS}	Address Setup Time		116		ns
T_{AH}	Address Hold Time		423		ns
T_{DS}	Data Setup Time		298		ns
T_{DH}	Data Hold Time		61		ns
T_{WP}	BPWR# Pulse Width		270		ns

Flash Read Timing

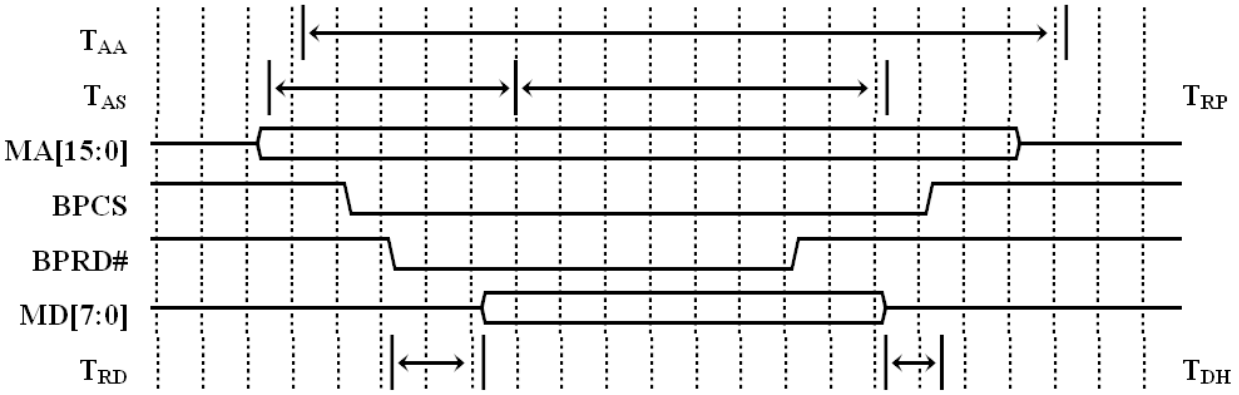


Figure 16. Flash Read Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_{AS}	Address Setup Time		85		ns
T_{AA}	Address Cycle Time		508		ns
T_{RP}	BPWR# Pulse Width		330		ns
T_{RD}	Read Access Time			230	ns
T_{DH}	Data Hold Time			0	ns

LED Display

LED On / Off (0 < Tpd < 300)

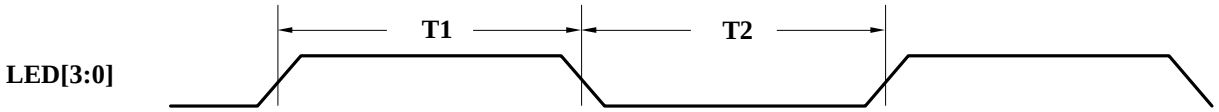


Figure 17. LED On / Off (0 < Tpd < 300)

Symbol	Parameter	Min	Typ	Max	Unit
T_1	LED[3:0] On Time		68		ms
T_2	LED[3:0] Off Time		68		ms

TP Interface

10BaseT Normal Link Pulse Timing (0 < Tpd < 300)

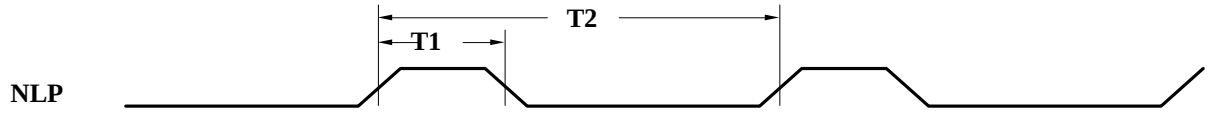


Figure 18. 10Base-T Normal Link Pulse Timing (0 < Tpd < 300)

Symbol	Parameter	Min	Typ	Max	Unit
T_1	NLP Pulse Width		100		ns
T_2	NLP TO NLP Period		12		ns

Auto Negotiation Fast Link Pulse Timing (0 < Tpd < 300)

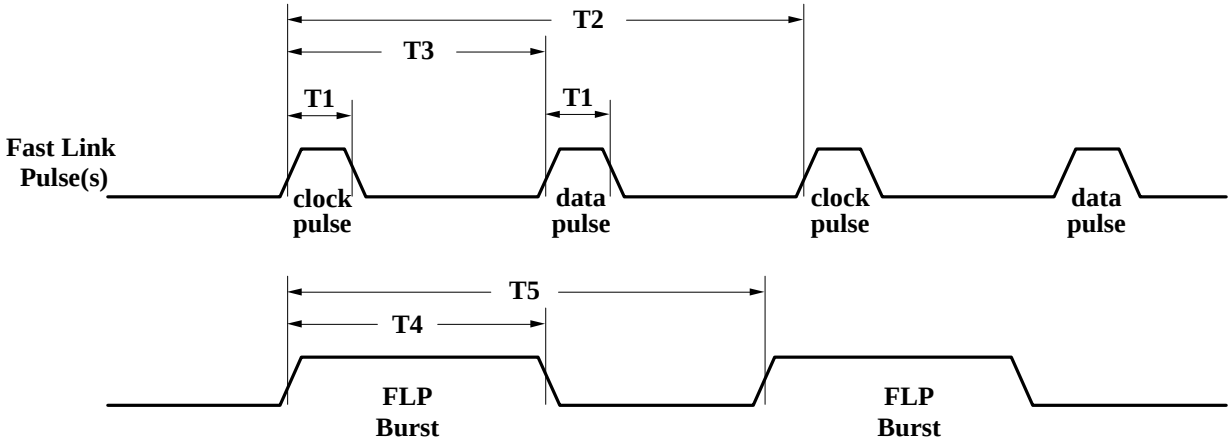


Figure 19. Auto Negotiation Fast Link Pulse Timing (0 < Tpd < 300)

Symbol	Parameter	Min	Typ	Max	Unit
T_1	Clock, Data Pulse Width		100		ns
T_2	Clock Pulse to Clock Pulse Period		125		µs
T_3	Clock Pulse to Data Pulse Period		62.5		µs
T_4	Burst Width		4.2		ns
T_5	FLP Burst to FLP Burst Period		8.5		ns

Running State Software Driven Internal PHY Reset Timing:

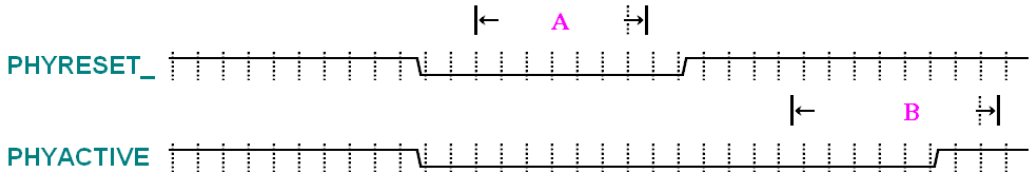
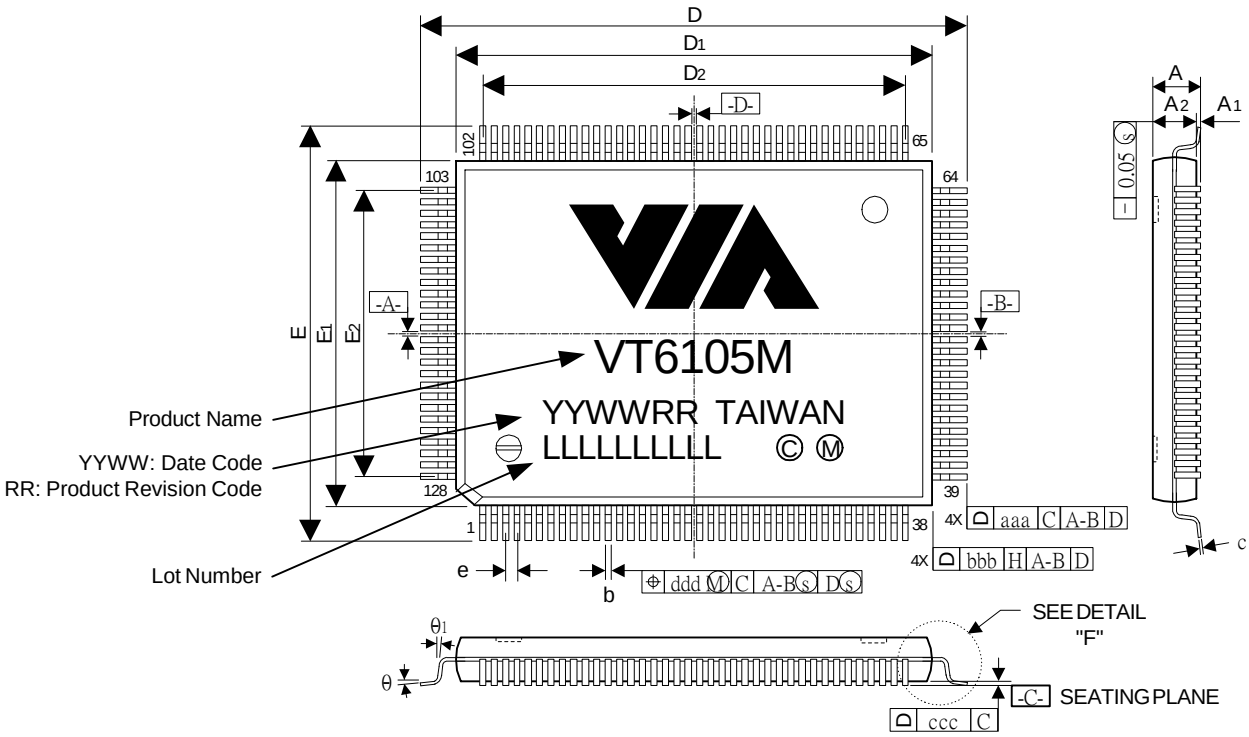
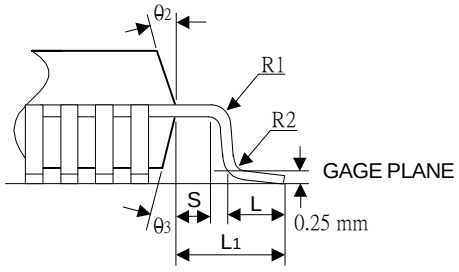


Figure 20. Running State Software Driven Internal PHY Reset Timing

Item	Description	Min	Max	Unit
A	Clock, Data Pulse Width	10		us
B	VT6105 PHY can begin to accept MDIO cycle after software initiated PHY Reset is de-asserted.	30 1		cyc uS

MECHANICAL SPECIFICATIONS





DETAIL "F"

NOTES :

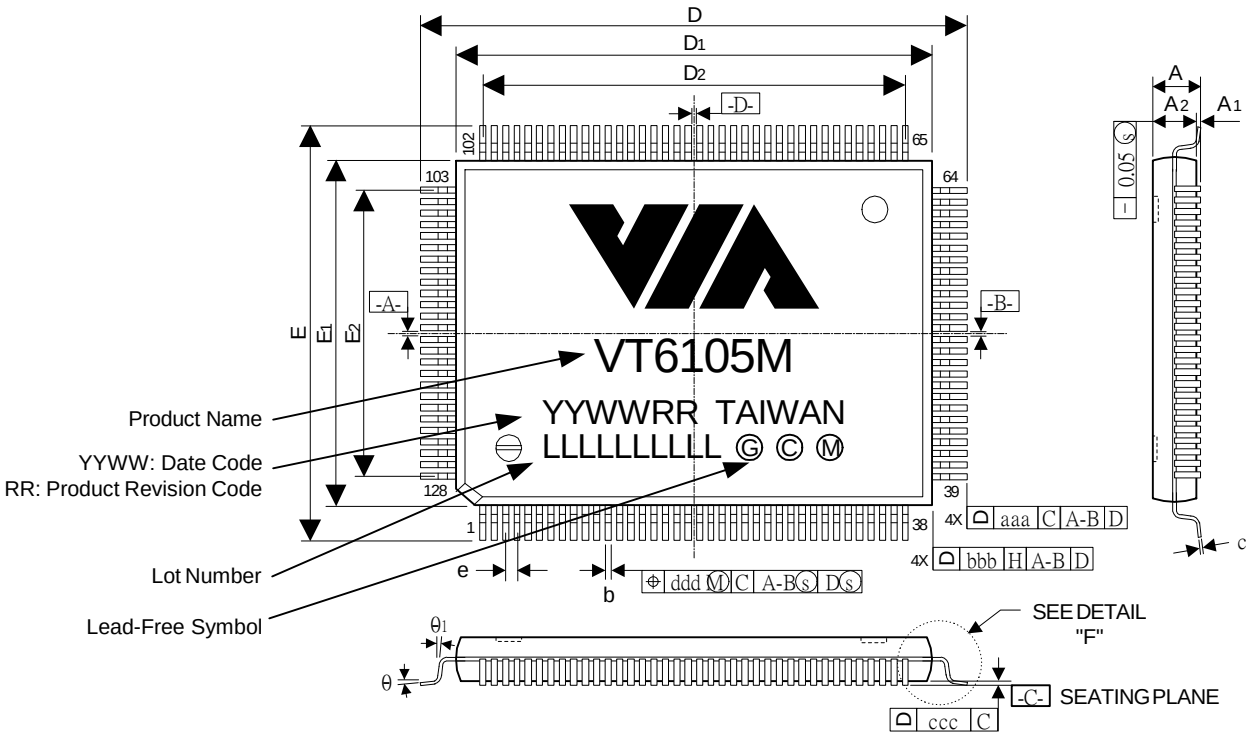
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

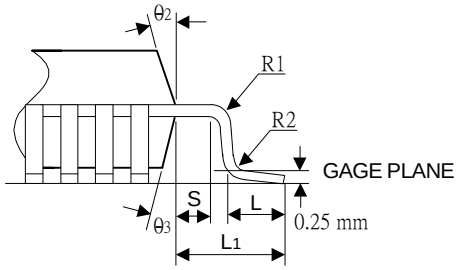
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
E	17.20 BASIC			0.677 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.13	—	0.30	0.005	—	0.012
R2	0.13	—	—	0.005	—	—
θ	0	—	7	0	—	7
θ1	0	—	—	0	—	—
θ2	15 REF			15 REF		
θ3	15 REF			15 REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 21. PQFP-128 Package (14 × 20 mm)





DETAIL "F"

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
E	17.20 BASIC			0.677 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.13	—	0.30	0.005	—	0.012
R2	0.13	—	—	0.005	—	—
θ	0	—	7	0	—	7
θ1	0	—	—	0	—	—
θ2	15 REF			15 REF		
θ3	15 REF			15 REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 22. Lead-Free PQFP-128 Package (14 × 20 mm)