Data Sheet

VT6130

PCI Express Gigabit Ethernet Controller

with

ACPI and Management Functions

Preliminary Revision 1.0
November 28, 2008

VIA TECHNOLOGIES, INC.

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VT6130

Gigabit Ethernet Controller for PCI Express

PRODUCT FEATURES

Key Features

- Fully IEEE 802.3, 802.3u (10BASE-T, 100BASE-TX), 802.3ab (1000BASE-T) & 802.3z (1000BASE-X) compliant
- Supports half / full duplex mode and 802.3x Flow Control
- 2 build-in linear regulator to generate 2.1 and 1.2 Voltage
- Automatic detection & correction of cable pair swaps, pair skew, & pair polarity, along with an Auto MDI/MDI-X crossover function
- Built-in integrated oscillator circuit
- Four direct drive LED pins with programmable LED modes
- Low EMI line drivers with robust CESD performance

Bus Architecture

- Compliance to PCI Express Rev1.1
- Supports Advanced Error Reporting capability
- Active State Power Management (ASPM) to L0s and L1
- PCIe Bus master Dual Channel DMA support for Tx/Rx
- Tx/Rx descriptor Scatter and Gather support in host memory
- No Transmit data byte alignment restriction, Rx data buffer should be double word alignment
- Flexible programmable max read request sizes and advanced internal arbitration control to optimize the bus utilization
- 256 bytes IO map/ 256 bytes memory map IO range in 32-bit/64-bit addressing
- 64-bit addressing Option in slave mode is loading from EEPROM
  - Bus Slave support 64-bit addressing
  - Use global Descriptor DMA and FIFO DMA Hi-16 bit address
- Adaptive interrupt service scheme for interrupt Coalescence

Network Functionality

- 64 x 48 CAM for 32 perfect filtering & 32 interest packet perfect filtering
- Supports jumbo frames up to 8KB
- Integrates on-chip TX and RX FIFO for high performance application

Network Management

- WFM2.0 enable for server
- SNMP-management, DMI2.0, PXE2.1
- Advanced Configuration Power management Interface (ACPI), Wake On Lan and Microsoft onNow
- Supports PCI Message Signaled Interrupt (MSI)
- PCI PMU1.1
- 802.1Q VLAN, 64x12 CAM VLAN ID perfect filtering
  - Long frame support (1518 + 4)
  - VLAN tag insertion for transmit packets
  - VLAN tag detection and removal for receive packets.

- 802.1Q 8-level priority transmit and receive (MAC support 4 TD, 1 RD queue)
- CheckSum offload
  - Ipv4 checksum task offload
  - IP forms are EtherType = 0800h, IEEE 802.2, and SNAP
  - IEEE 802.1Q compliant VLAN are supported
  - Fragmented IP datagrams are not supported
  - Tx checksum generation for IP (IP option), TCP, and UDP
  - Rx checksum validation for IP (IP option), TCP, and UDP
- Statistics for RFC1213 (MIBII) RFC1398 (etherLike MIB) 802.3 LME
- Large Packet Segmentation Offload

Misc. Support

- 64-word nm93c46 serial ROM interface, support
  - Embedded random word access
  - Dynamic and power up Loading to update chip default configuration
  - Software driven direct programming
- Supports Shadow-EEPROM function to work without external EEPROM device
  - Built-in 20-word shadow memory to store EEPROM data
- SPI BROM Interface
- PVDET as PCI power detection
- Supports 4 modes LED behavior (4 LED pins)
- Built-in linear power regulator to simplify power partition on board

Advance Software Support

- Adaptive Load Balance

Technology

- 0.15 um low voltage process
- 1.2V core power and 3.3V / 2.5V IO power with 5V tolerant inputs
- QFN-64 package

System Application.

- Desktop and Server NICs
- LAN-on-Motherboard and Mobile PC NICs

OVERVIEW

VT6130 supports standard IEEE 802.3 Ethernet operations with 10/100/1000-Mbps triple-speed and full/half-duplex capability at all speeds. The integrated PHY is fully compliant to IEEE 802.3 (10BASE-T), 802.3u (100BASE-TX), and 802.3ab (1000BASE-T) standards.

To maximize media-side traffic throughput, VT6130 provides on-chip RAM to enable an efficient data buffering and maintain high performance as available PCI bandwidth changes. On the other hand, to minimize host-side CPU utilization, the devices adopt an adaptive interrupt scheme to reduce interrupts called to CPU, and maximize the use of packet bursts. The devices can also offload tasks from the host CPU to further improve the overall system performance. Both the TCP/UDP/IP checksum offloading and TCP segmentation offloading are supported.

VT6130 fully incorporates with advanced power management schemes, such as PCI Power Management v1.1 and ACPI v2.0. This enables energy-efficient operations and lowers the power consumption. The devices can support multiple wake-up events through the detection of Magic packet, Interesting Pattern Match packets or Link Status changes. Two special events not defined in Wake-on-LAN standard, the AC Power Loss and PCI Abnormal Shut-Down Wake-Up, are also supported by detecting Magic packet. The devices also support other legacy Wake-on-LAN cases.

To further reduce system complexity and cost, user can select to power the devices from a single 3.3V power supply by utilizing the devices' on-chip regulator circuits to produce 2.1V and 1.2V core power supply.

The delivery of VT6130 also comes with a software suite GigaCheck™, a complete set of drivers, diagnostic utilities and management software program. These devices provide customers with outstanding performance, low power and cost-effective PCI Express Gigabit Ethernet solutions.

Packaged in a small form factor 64-pin QFN (9x9 mm), the VT6130 device is optimized for LAN on Motherboard (LoM) applications of desktop and notebook.

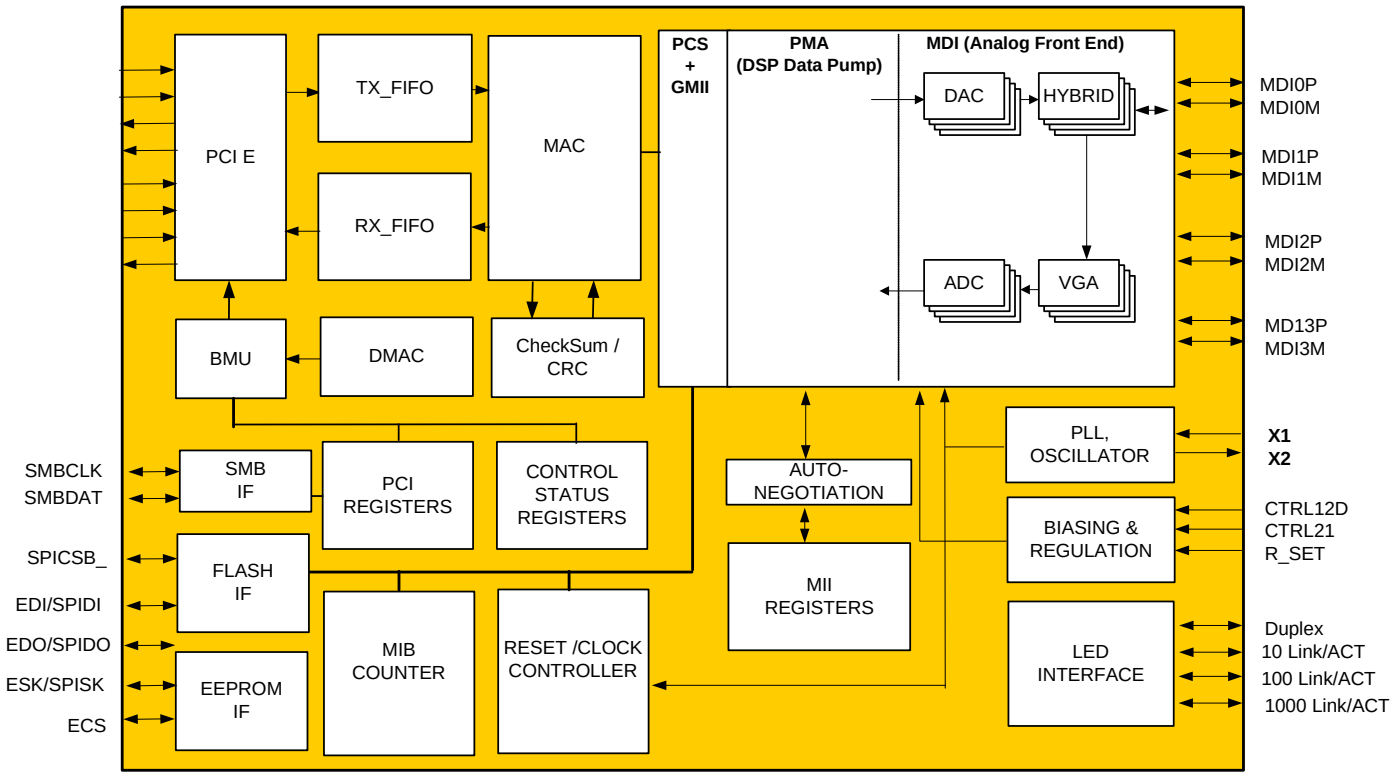


Figure 1. Internal Block Diagram

PINOUT

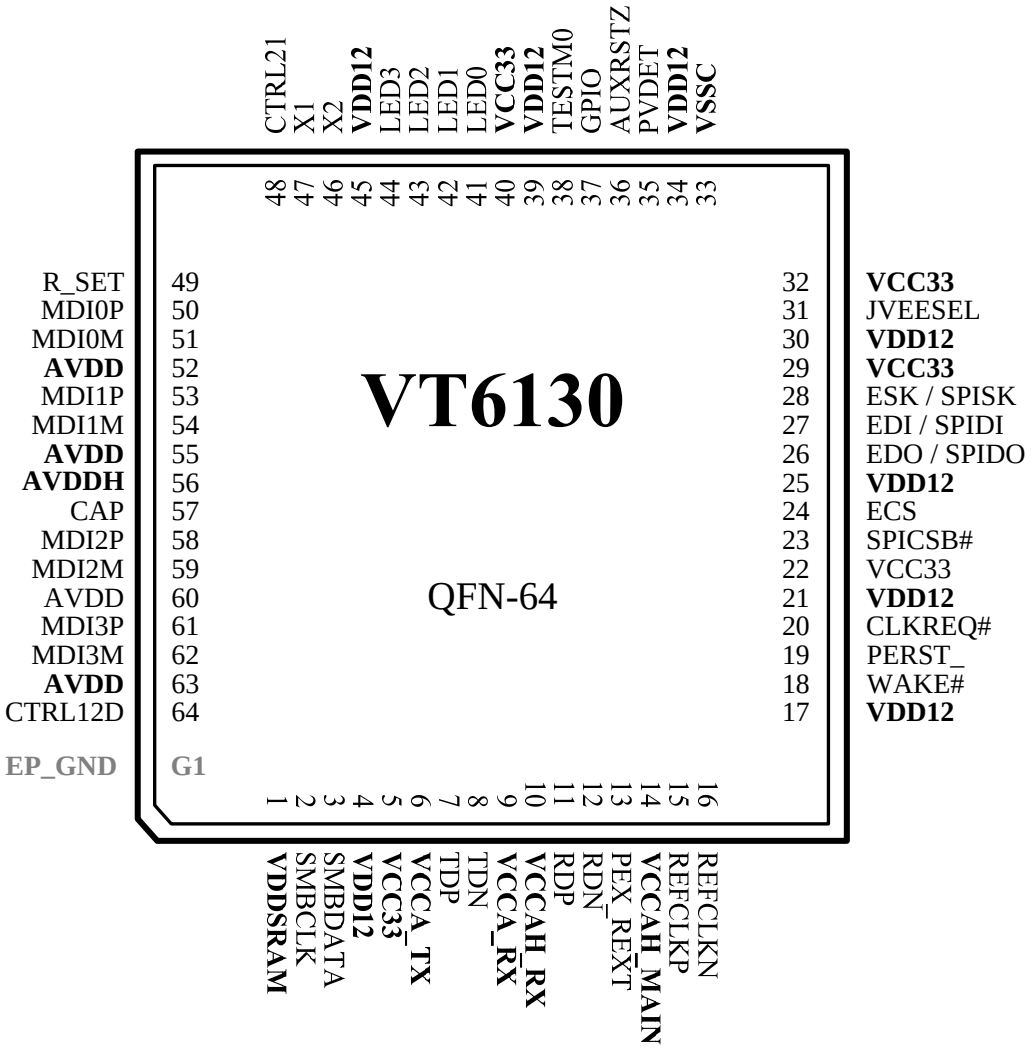


Figure 2. Pin Diagram

Table 1. Pin List

No.	Name	No.	Name
36	AUXRSTZ	12	RDN
52	**AVDD**	11	RDP
55	**AVDD**	16	REFCLKN
60	**AVDD**	15	REFCLKP
63	**AVDD**	2	SMBCLK
56	**AVDDH**	3	SMBDATA
57	CAP	23	SPICSB#
20	CLKREQ#	8	TDN
64	CTRL12D	7	TDP
48	CTRL21	38	TESTM0
24	ECS	5	**VCC33**
27	EDI / SPIDI	22	**VCC33**
26	EDO / SPIDO	29	**VCC33**
28	ESK / SPISK	32	**VCC33**
37	GPIO	40	**VCC33**
31	JVEESEL	9	**VCCA_RX**
41	LED0	6	**VCCA_TX**
42	LED1	14	**VCCAH_MAIN**
43	LED2	10	**VCCAH_RX**
44	LED3	4	**VDD12**
51	MDI0M	17	**VDD12**
50	MDI0P	21	**VDD12**
54	MDI1M	25	**VDD12**
53	MDI1P	30	**VDD12**
59	MDI2M	34	**VDD12**
58	MDI2P	39	**VDD12**
62	MDI3M	45	**VDD12**
61	MDI3P	1	**VDDSRAM**
19	PERST_	33	**VSSC**
13	PEX_REXT	18	WAKE#
35	PVDET	47	X1
49	R_SET	46	X2
G1	EP_GND		

Table 2. Signal Type Definitions

Type	Description
I	**Input.** Standard input-only signal.
O	**Output.** Standard active output driver.
I/O	**Input/output.** An input/output signal.
T/S	**Tri-state.** Inactive bi-directional input/output pin.
OD	**Open drain.** Allows multiple devices to share as a wire-OR.
A_{DIFF}	**Analog differential.** Signal pair for the twisted-pair interface.
A_{BIAS}	**Analog bias or reference signal.** Must be tied to external resistor and/or capacitor bias network, as shown in the system schematic.

Pin Descriptions

Table 3. Pin Descriptions

PCI Express Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TDP **TDN**	7 8	A_{DIFF}	**PCI Express Transmitter Differential Pair.**
RDP **RDN**	11 12	A_{DIFF}	**PCI Express Receiver Differential Pair.**
REFCLKP **REFCLKN**	15 16	I	**PCI Express Differential Clock.** The PCI Express externally provided differential clock with 100Mhz +- 300ppm. Spread Spectrum Clocking (SSC) is allowed
PERST_	19	I	**PCI Express Reset.** When PERST_ is asserted low, the chip performs an internal system hardware reset. PERST_ may be asynchronous to CLK asserted or deasserted. It is recommended that the deassertion be synchronous to guarantee clean and bounce free edge. The PERST_ assertion/deassertion should meet the timing spec defined in PCI Express Card Electromechanical Specification Revision 1.1a.
CLKREQ#	20	OD	**Clock Request.** When CLKREQ# is disabled, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked clock state. The CLKREQ# assertion/ deassertion is asynchronous to reference clock and should meet the timing spec defined in PCI Express Card Electromechanical Specification Revision 1.1

SMBus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SMBCLK	2	O/D	**SMBus Interface Clock.**
SMBDATA	3	O/D	**SMBus Interface Data.**

Local Memory Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
JVEESEL	31	O	**Virtual EEPROM Selection.**
ECS	24	O	**EEPROM Chip Select.** Chip select signal of the external EEPROM
EDI / SPIDI	27	O	**EEPROM Data In.** External serial EEPROM data input.
EDO / SPIDO	26	I	**EEPROM Data Out.** External serial EEPROM data output.
ESK / SPISK	28	O	**EEPROM Clock.** External serial EEPROM clock

SPI Flash Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SPICSB#	23	O	**SPI Flash Chip Select.** Chip select signal of the external SPI Flash.
SPIDI / EDI	27	O	**SPI Flash Data In.** External SPI Flash data input.
SPIDO / EDO	26	I	**SPI Flash Data Out.** External SPI Flash data output.
SPISK / ESK	28	O	**SPI Clock.** External SPI Flash clock

Media Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MDI0P, MDI0M	50, 51	I/O	**Twisted-Pair Media Dependent Interface.** In 1000BASE-T mode, all 4 pairs are both input and output at the same time. In 100BASE-TX and 10BASE_T modes: MDI0P/MDI0M are used for transmit pair under MDI configuration and for receive pair under MDIX configuration. MDI1P/MDI1M are used for receive pair under MDI configuration and for transmit pair under MDIX configuration. In 100BASE-TX and 10BASE-T modes: MDI2P/MDI2M and MDI3P/MDI3M are unused.
MDI1P, MDI1M	53, 54		
MDI2P, MDI2M	58, 59		
MDI3P, MDI3M	61, 62		

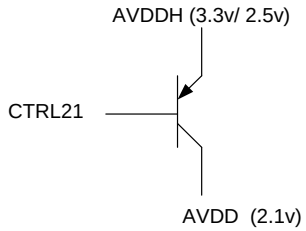
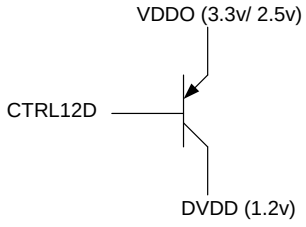
LED Status Output			
Signal Name	**Pin #**	**I/O**	**Signal Description**
LED0	41	O	**LED Status Outputs.** Output pins for directly driving status LEDs. When enabled by SMI register bit 27.3, all LED outputs are pulsed at 5kHz with a 20% duty cycle for low-power operation.
LED1	42		
LED2	43		
LED3	44		

Power Management Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
WAKE#	18	OD	**System WakeUp.** This signal is asserted low to reactivate the PCI Express slot's main power rails and reference clocks.

System Clock Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
X1	47	I	**Crystal Input.** The reference input clock is 25MHz, with a +50ppm frequency tolerance or connected to a 25MHz, parallel resonant crystal with a +50ppm frequency tolerance. When used with a crystal, a 33pF capacitor is connected from this pin to ground.
X2	46	O	**Crystal Output.** 25MHz parallel resonant crystal output. A 33pF capacitor is connected from this output to ground.

Miscellaneous Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TESTM0	38	I	Operation mode setting 0.
AUXRSTZ	36	I	External RC for suspend power on reset for testing purpose.
GPIO	37	I/O	General Purpose Input and Output.
PVDET	35	I	Schmit-trigger tied down input, used for global single power design approach to monitor PCI power.

Regular Control and Analog Bias Pins			
Signal Name	**Pin #**	**I/O**	**Signal Description**
R_SET	49	A_{BIAS}	**Band Gap Reference.** Add an external 6.2 ±1% KΩ resistor between this pin and GND. VT6130 utilizes this resistor to set the current source.
PEX_REXT	13	A_{BIAS}	**Bias** pin to external 5.6KΩ (1%) resistor tied to analog ground.
CAP	57	P	Connected to an external Capacitor. It is used to stable internal 1.2V power source.

Regular Control and Analog Bias Pins (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
CTRL21	48	O	**Regular Control**. The internal linear regulator uses this pin to control an external PNP transistor to generate a 2.1V voltage source. VT6130 uses the AVDDH as a reference voltage, which can be 3.3V or 2.5V as shown in the following figure. The 2.1V power source is used for center tap of transformer and AVDD. The built-in regulator works only if AVDD pins are connected to the collector of the external PNP as shown in the following figure. If AVDD pins are connected an external power source instead of the collector of PNP, the function of CTRL21 doesn't work. 
CTRL12D	64	O	The internal linear regulator uses this pin to control an external PNP transistor to generate a 1.2V voltage source. VT6130 uses the VCC33 as a reference voltage, which can be 3.3v or 2.5v as shown in the following figure. The 1.2V power source is used for VDD12. The built-in regulator works only when VDD12 pins are connected to the collector of the external PNP as shown in the following figure. If VDD12 pins are connected an external power source instead of the collector of PNP, the function of CTRL12D doesn't work. 

Analog Power Supply			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AVDD	52, 55, 60, 63	P	**GEPHY RX/TX Power Supply** (2.1V).
AVDDH	56	P	**GEPHY High Voltage Input** (3.3V / 2.5V).
VCCA_TX	6	P	**PCIe PHY TX Power Supply** (1.2V)
VCCA_RX	9	P	**PCIe PHY RX Power Supply** (1.2V).
VCCAH_RX	10	P	**PCIe PHY RX Power Supply** (3.3V).
VCCAH_MAIN	14	P	**PCIe PHY Power Supply** (3.3V).

Digital Power Supply Signal Description			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC33	5, 22, 29, 32, 40	P	**I/O Power Supply** (3.3V)
VDD12	4, 17, 21, 25, 30, 34, 39, 45	P	**Core Power Supply** (1.2V)
VSSC	33	G	**Core Ground.**
VDDSRAM	1	P	**SRAM Power** (+1.2V ± 5%)
EP_GND	G1	P	**QFN Package Ground**

REGISTER OVERVIEW

Abbreviation

Listed in the table below are the abbreviations of register access types and its abbreviation implemented for the registers.

Access Type	Description
R	Read
W	Write
R/W	Read/Write
R0	Read as Zero
RO	Read Only
W0	Write "1" clear by software
W1	Write "1" set by software
E	Updated by EEPROM loading
U	Updated by Hardware Controller
C/S	Clear or set by Hardware Controller
HC	Hardware Control
LH	Latched High
LL	Latched Low
SC	Software Driver Control
HW Reset	Reset by RESET_ pin
SW Reset	Reset by MII Register 0[15]
N/A	Not affected

Register Map Tables

PCI Configuration Register Mapping

Table 4. PCI Configuration Register Map

Device ID			Vendor ID								**00h**
Status			Command								**04h**
CLASS_CODE								Rev ID			**08h**
BIST	Header Type		LAT Timer					Cache Line			**0Ch**
CSR IO Mapped Base Addr (256Byte) 000						0	0	0	0	1	**10h**
CSR MEM Mapped Base Addr (256Byte) 000						0	0	E	0	0	**14h**
CSR MEM Mapped Base Addr High Address											**18h**
32'h0											**20h**
32'h0											**24h**
32'h0											**28h**
SUB System ID			SUB Vendor ID								**2Ch**
Expansion ROM Base Address [31:13]				12'h0						E	**30h**
00 0000h								Capability Pointer			**34h**
Max_LAT	Min_GNT		INT PIN					4h'0		INTLN [3:0]	**3Ch**
Reserved											**40 - 4Fh**
PMU Capability											
PMC(fr EE)			Next Pointer					01h			**50h**
DATA(00)	BSE(00)h		S	0000000	E			000000		WS*	**54h**
32'h0											**58h**
	VEE_CTL			Raddr		VEE_Read_Port					**5Ch**
Reserved											**60h**
Reserved											**64h**
xDevID			XVenID								**68h**
PCI Express Capability Structure											
PCI Express Capability			Next Pointer					10h			**90h**
Device Capability											**94h**
Device Status			Device Control								**98h**
Link Capability											**9Ch**
Link Status			Link Control								**A0h**
MSI Capability Structure											
MSI Control			Next Pointer					05h			**C0h**
MSI Low Address											**C4h**
MSI High Address											**C8h**
16'h0			Message Data								**CCh**
MSI MSK											**D0h**
MSI PEND											**D4h**

Note:
WS: If software wants to write a power state that the chip does not support, the write cycle will be granted but discarded internally.

Table 5. PCI Express Extended Capabilities Structure (> FF h)

Advanced Error Reporting Capabilities Structure			
Next Capability Offset	Cap Ver	Extended Capability ID	**1_00h**
Uncorrectable Error Status			**1_04h**
Uncorrectable Error Mask			**1_08h**
Uncorrectable Error Severity			**1_0Ch**
Correctable Error Status			**1_10h**
Correctable Error Mask			**1_14h**
Advanced Error Capability and Control			**1_18h**
Header Log of TLP			**1_1Ch**
Header Log of TLP			**1_20h**
Header Log of TLP			**1_24h**
Header Log of TLP			**1_28h**
Device Serial Number Enhanced Capabilities Structure			
Next Capability Offset	CapVer	Extended Capability ID	**1_30h**
Device Serial Number [31:0]			**1_34h**
Device Serial Number [63:32]			**1_38h**

Control and Status Registers Mapping

VT6130 provides 256 bytes space range with some page selection in some offset on PCI IO Map and Memory mapped IO space, defined in PCI configuration space 1x10h and 0x14h. In Windows and gigabit VGHCI, a memory mapped IO based software is preferred. The IO space addressing is defined to be 32-bit IO read/write cycles.

Global Control & ID

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
00	PAR3	PAR2	PAR1	PAR0
04	TCR	RCR	PAR5	PAR4
08	CR3.S	CR2.s	CR1.s	CR0.s
0C	CR3.c	CR2.c	CR1.c	CR0.c
10	MAR3/CAM	MAR2/CAM	MAR1/CAM	MAR0/CAM
14	MAR7/CAM	MAR6/CAM	MAR5/CAM	MAR4/CAM
18	DescBaseAddr.Hi[63:32]			
1C	Reserved		DataBufBaseAddr.Hi[63:48]	

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
20	RXE_SR	TXE_SR	ISR_CTL	
24	ISR3	ISR2	ISR1	ISR0
28	IMR3	IMR2	IMR1	IMR0
2C	TD_STATUS_PORT			
30		RDCSR0.s[3:0]	TDCSR1.s	TDCSR0.s
34		RDCSR0.c[3:0]	TDCSR1.c	TDCSR0.c
38	RDBase0.Lo[31:6]			
3C	RQETMR	TQETMR	RDINDX	

Receive Desc DMA Register for Debugging Purpose

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
40	TDBase0.Lo[31:6]			
44	TDBase1.Lo[31:6]			
48	TDBase2.Lo[31:6]			
4C	TDBase3.Lo[31:6]			
50	TDCSIZE[11:0]		RDCSIZE	
54	TDIDX1[11:0]		TDIDX0[11:0]	
58	TDIDX3[11:0]		TDIDX2[11:0]	
5C	RBRDU		Tx Pause Timer	

Configuration /Misc Register

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
60	Reserved			
64	Reserved			
68	Reserved	Reserved	CAMCR	CAMADDR
6C	Reserved	PHYSR0	MIISR	MIICFG
70	MII DATA PORT		MIIADR	MIICR
74	SOFT TIMER 1		SOFT TIMER 0	
78	CFGD	CFGC	CFGB	CFGA
7C	MCFG1	MCFG0	DCFG1	DCFG0

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
80	STICKHW	PMCPORT	Reserved	
84	Reserved		EE_SWDAT	MIBCR
88	MIB READ PORT			
8C	BPMD w	BPMAHHi	BPMA/EE_WR_DATA	
90	EECSR	CHKSUM	BPMD_r	BPCMD
94	EMBCMD	EADDR	EE_RD_DATA	
98	MJMPSR	CJMPSR2	JMPSR1	JMPSR0
9C	CHIP_GCR	Reserved	Reserved	CHIP_GSR

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
A0	WOLCFG.s	PWCFG.s	WOLCR1.s	WOLCR0.s
A4	WOLCFG.c	PWCFG.c	WOLCR1.c	WOLCR0.c
A8	Reserved		WOLSR1.s	WOLSR0.s
AC	Reserved		WOLSR1.c	WOLSR0.c
B0	PATTERN_CRC1[15:0]		PATTERN_CRC0[15:0]	
B4	PATTERN_CRC3[15:0]		PATTERN_CRC2[15:0]	
B8	PATTERN_CRC5[15:0]		PATTERN_CRC4[15:0]	
BC	PATTERN_CRC7[15:0]		PATTERN_CRC6[15:0]	

WAKE-UP PATTERN MASK1,2,3,4, also Used to Store Firmware

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
C0	Pattern 0/4, PTNBMSK[31:0]			
C4	Pattern 0/4, PTNBMSK[63:32]			
C8	Pattern 0/4, PTNBMSK[95:64]			
CC	Pattern 0/4, PTNBMSK[127:96]			
D0	Pattern 1/5, PTNBMSK[31:0]			
D4	Pattern 1/5, PTNBMSK[63:32]			
D8	Pattern 1/5, PTNBMSK[95:64]			
DC	Pattern 1/5, PTNBMSK[127:96]			
E0	Pattern 2/6, PTNBMSK[31:0]			
E4	Pattern 2/6, PTNBMSK[63:32]			
E8	Pattern 2/6, PTNBMSK[95:64]			
EC	Pattern 2/6, PTNBMSK[127:96]			
F0	Pattern 3/7, PTNBMSK[31:0]			
F4	Pattern 3/7, PTNBMSK [63:32]			
F8	Pattern 3/7, PTNBMSK [95:64]			
FC	Pattern 3/7, PTNBMSK [127:96]			

MII Register Mapping Table

Table 6. MII Registers Names & Addresses

Register Number	Register Address	Register Name
0	00	Mode Control
1	01	Mode Status
2	02	PHY Identifier Register #1
3	03	PHY Identifier Register #2
4	04	Auto-Negotiation Advertisement
5	05	Auto-Negotiation Link Partner Ability
6	06	Auto-Negotiation Expansion
7	07	Auto-Negotiation Next-Page Transmit
8	08	Auto Negotiation Link Partner Next Page
9	09	1000BASE-T Control
10	0A	1000BASE-T Status
14 - 11	0E - 0B	Reserved
15	0F	Extended Status
16	10	PHY Specific Control Register #1
17	11	PHY Link Status
19 - 18	13 - 12	Reserved
20	14	PHY Specific Control Register #2
31 - 21	1F - 1E	Reserved

REGISTER DESCRIPTIONS

PCI Configuration Space

Header Register (Offset 00 – 3Fh)

Offset 01h – 00h: Vender ID

Offset 03h – 02h: Device ID

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:16	RW	RO	3119h	**Device ID**
15:0	RW	RO	1106h	**Vender ID**

Offset 05h – 04h: Device Command

Bit	Attribute		Default	Description
	SMBus	PCIe		
15:11	RO	RO	0	**Reserved**
10	RW	RW	0	**Interrupt Disable**
9	RO	RO	0	**Fast Back-to-Back Enable**
8	RW	RW	0	**SERR Enable**
7	RO	RO	0	**IDSEL Stepping**
6	RW	RW	0	**Parity Error Enable**
5	RO	RO	0	**VGA Palette Snoop**
4	RO	RO	0	**Memory Write and Invalidate**
3	RO	RO	0	**Special Cycle Enable**
2	RW	RW	0	**Bus Master Enable**
1	RW	RW	0	**Memory Space**
0	RW	RW	0	**IO Space**

Offset 07h – 06h: Device Status

Bit	Attribute		Default	Description
	SMBus	PCIe		
15	RO	RW1C	0	**Detected Parity Error**
14	RO	RW1C	0	**Signaled System Error**
13	RO	RW1C	0	**Received Master Abort**
12	RO	RW1C	0	**Received Target Abort**
11	RO	RW1C	0	**Signaled Target Abort**
10:9	RO	RO	0	**DEVSEL Timing**
8	RO	RW1C	0	**Master Data Parity Error**
7	RO	RO	0	**Fast Back-to-Back Transaction Cap**
6	RO	RO	0	**Reserved**
5	RO	RO	0	**66MHz Capable**
4	RO	RO	1b	**Capabilities List**
3	RO	RO	0	**Interrupt Status**
2:0	RO	RO	0	**Reserved**

Offset 0Bh – 08h: Device Identification

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:8	RO	RO	02 0000h	**Class Code**
7:0	RO	RO	82h	**Revision ID**

Offset 0Fh – 0Ch: Misc Registers

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:24	RO	RO	0	**BIST**
23:16	RO	RO	0	**Header Type**
15:8	RO	RO	0	**Master Latency Timer**
7:0	RW	RW	0	**Cache Line Size**

Offset 13h – 10h: CSR IO Mapping Base Address

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:8	RW	RW	0	**IOBASE**
7:0	RO	RO	01h	

Offset 17h – 14h: CSR Memory Mapping Base Address

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:8	RW	RW	0	**Memory Mapping Base Address [31:8]**
7:3	RO	RO	0	**Reserved**
2	RE	RE	0	**MMIO32_64**
1:0	RO	RO	0	**Reserved**

Offset 1Bh – 18h: CSR Memory Mapped Base Address - High

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:0	RW	RW	0	**Memory Mapping Base Address [63:32].** Write when MMIO32_64 (offset 14h[2]) asserted.

Offset 2Dh – 2Ch: Subsystem Vendor ID

Bit	Attribute		Default	Description
	SMBus	PCIe		
15:0	RE	RE	1106h	**Subsystem Vendor ID**

Offset 2Fh – 2Eh: Subsystem ID

Bit	Attribute		Default	Description
	SMBus	PCIe		
15:0	RE	RE	0130h	**Subsystem ID**

Offset 33h – 30h: Expansion ROM Base Address

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:13	RU	RU	0	**EXPROM**
12:1	RO	RO	0	**Reserved**
0	RU	RU	0	**ROMBSEN**

Offset 34h: Capability Pointer

Bit	Attribute		Default	Description
	SMBus	PCIe		
7:0	RO	RO	50h	**Capability Pointer**

Offset 3Bh – 35h: Reserved

Offset 3Fh – 3Ch: Misc Registers

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:24	RO	RO	0	**Max_LAT**
23:16	RO	RO	0	**Min_GNT**
15:8	RO	RO	01h	**Interrupt Pin (INTA)**
7:0	RW	RW	00h	**Interrupt Line**

PMU Capabilities (Offset 50 – 5Fh)

Offset 53h – 50h: PM Capability

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:27	RO	RO	01h	**PME Support**
26	RO	RO	1b	**D2 Support**
25	RO	RO	1b	**D1 Support**
24:22	RO	RO	010b	**AUX Current**
21	RO	RO	0	**Device Specific Initialization (DSI)**
20:19	RO	RO	0	**Reserved**
18:16	RO	RO	03h	**Version**
15:8	RO	RO	90h	**Next PTR**
7:0	RO	RO	01h	**Capability ID**

Offset 57h – 54h: PM Status Control

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:24	RO	RO	0	**Data**
23:16	RO	RO	0	**Reserved**
15	RO	RW1CS	0	**PME Status**
14:13	RO	RO	0	**Data Scale**
12:9	RW	RW	0	**Data Select**
8	RWS	RWS	0	**PME Enable**
7:4	RO	RO	0	**Reserved**
3	RW	RO	0	**NO_SFRST**
2	RO	RO	0	**Reserved**
1:0	RW	RW	0	**Power State**

Offset 5Fh – 5Ch: VMSTS, VEEPDO

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:28	RO	RO	0	**Reserved**
27	RW	RW	0	**R_ERDBG**
26	RO	RO	0	**Reserved**
25	RU	RU	0	**P_SEELD**
24	RU	RU	0	**P_SEEPR**
23:21	RO	RO	0	**Reserved**
20:16	RW	RW	0	**VMRADR**
15:0	RO	RO	0	**VEEPDO**

Offset 67h – 60h: Reserved

Offset 69h – 68h: xVenID

Bit	Attribute		Default	Description
	SMBus	PCIe		
15:0	RO	RO	1106h	**xVenID**

Offset 6Bh – 6Ah: xDevID

Bit	Attribute		Default	Description
	SMBus	PCIe		
15:0	RO	RO	3119h	**xDevID**

PCI Express Capability Structure (Offset 90 – A3h)

Offset 93h – 90h: PCI Express Capability

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:30	RO	RO	0	**Reserved**
29:25	RO	RO	0	**Interrupt Message Number**
24	RO	RO	0	**Slot Implemented**
23:20	RW	RO	1h EEPROM	**Device/Port Type**
19:16	RO	RO	1h	**Capability Version**
15:8	RO	RO	C0h	**Next Pointer**
7:0	RO	RO	10h	**Capability ID**

Offset 97h – 94h: PCI Express – Device Capability

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:28	RO	RO	0	**Reserved**
27:26	RO	RO	0	**Captured Slot Power Limit Scale**
25:18	RO	RO	0	**Captured Slot Power Limit Value**
17:16	RO	RO	0	**Reserved**
15	RW	RO	1b	**RBEREN**
14	RO	RO	0	**Power Indicator Present**
13	RO	RO	0	**Attention Indicator Present**
12	RO	RO	0	**Attention Button Present**
11:9	RW	RO	0	**Endpoint L1 Acceptable Latency**
8:6	RW	RO	011b	**Endpoint L0s Acceptable Latency**
5	RO	RO	0	**Extended Tag Field Supported**
4:3	RO	RO	0	**Phantom Functions Supported**
2:0	RW	RO	0	**Maximum Payload Size Supported**

Offset 99h – 98h: PCI Express – Device Control

Bit	Attribute		Default	Description
	SMBus	PCIe		
15	RO	RO	0	**Reserved**
14:12	RW	RW	0	**Maximum Read Request Size**
11	RO	RO	0	**Enable No Snoop**
10	RW	RW	0	**AUX Power PM Enable**
9	RO	RO	0	**Phantom Functions Enable**
8	RO	RO	0	**Extended Tag Field Enable**
7:5	RW	RW	0	**Maximum Payload Size**
4	RO	RO	0	**Enable Relaxed Ordering**
3	RW	RW	0	**Unsupported Request Reporting Enable**
2	RW	RW	0	**Fatal Error Reporting Enable**
1	RW	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	RW	0	**Correctable Error Reporting Enable**

Offset 9Bh – 9Ah: PCI Express – Device Status

Bit	Attribute		Default	Description
	SMBus	PCIe		
15:6	RO	RO	0	**Reserved**
5	RO	RO	0	**Transaction Pending**
4	RO	RO	1b	**AUX Power Detected**
3	RW1C	RW1C	0	**Unsupported Request Detected**
2	RW1C	RW1C	0	**Fatal Error Detected**
1	RW1C	RW1C	0	**Non-Fatal Error Detected**
0	RW1C	RW1C	0	**Correctable Error Detected**

Offset 9Fh – 9Ch: PCI Express – Link Capability

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:24	RW	RO	0	**Port Number**
23:21	RO	RO	0	**Reserved**
20	RO	RO	0	**DLACT_RPT_CAP**
19	RO	RO	0	**SPRS_DOWN**
18	RW	RO	1b	**CLK_PM_CAP**
17:15	RW	RO	001b	**L1 Exit Latency**
14:12	RW	RO	100b	**L0s Exit Latency**
11:10	RW	RO	11b	**ASPM Support**
9:4	RO	RO	01h	**Maximum Link Width**
3:0	RO	RO	1h	**Maximum Link Speed**

Offset A1h – A0h: PCI Express – Link Control

Bit	Attribute		Default	Description
	SMBus	PCIe		
15:9	RO	RO	0	**Reserved**
8	RW	RW	0	**CFG_CLKREQEN**
7	RW	RW	0	**Extended Synch**
6	RW	RW	0	**Common Clock Configuration**
5:4	RO	RO	0	**Reserved**
3	RW	RW	0	**Read Completion Boundary (RCB)**
2	RO	RO	0	**Reserved**
1:0	RW	RW	0	**ASPM Control**

Offset A3h – A2h: PCI Express – Link Status

Bit	Attribute		Default	Description
	SMBus	PCIe		
15:14	RO	RO	0	**Reserved**
13	RO	RO	0	**DL_LNKACT**
12	RO	RO	1b	**Slot Clock Configuration**
11:10	RO	RO	0	**Reserved**
9:4	RO	RO	01h	**Negotiated Link Width**
3:0	RO	RO	1h	**Link Speed**

MSI Capability Structure (Offset C0 – D7)

Offset C3h – C0h: MSI Control Register Structure

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:25	RO	RO	0	**Reserved**
24	RW	RW	1b	**Per Vector Mask (PVM) Capable**
23	RO	RO	1b	**64-bit Address Capable**
22:20	RW	RW	0	**Multiple Message Enable**
19:17	RO	RO	0	**Multiple Message Capable**
16	RW	RW	0	**MSI Enable**
15:8	RO	RO	0	**Next Pointer**
7:0	RO	RO	05h	**Capability ID**

Offset C7h – C4h: MSI Low Address

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:2	RW	RW	0	**System-Specified Message Lower Address**
1:0	RO	RO	0	**Reserved**

Offset CBh – C8h: MSI High Address

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:0	RW	RW	0	**System-Specified Message Upper Address**

Offset CDh – CCh: MSI Data Register

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:16	RO	RO	0	**Reserved**
15:0	RW	RW	0	**System-Specified Message**

Offset D3h – D0h: MSI Mask

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:0	RW	RW	0	**The function is prohibited from generating the associated message for each mask bit that is set.**

Offset D7h – D4h: MSI Pending

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:1	RO	RO	0	**Reserved**
0	RO	RO	0	**PVM Pending Bit 0**

PCI Express Extended Space (Offset 1_1Ch – 1_00h)

Offset 1_03h – 1_00h: PCI Express – Advanced Error Reporting Enhanced Capability

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:20	RO	RO	0	**Next Capability**
19:16	RO	RO	1h	**Capability Version**
15:0	RO	RO	0001h	**PCI Express Extended Capability ID**

Offset 1_07h – 1_04h: PCI Express – Uncorrectable Error Status

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:21	RO	RO	0	**Reserved**
20	RW1CS	RW1CS	0	**Unsupported Request Error Status**
19	RW1CS	RW1CS	0	**ECRC Error Status (Optional)**
18	RW1CS	RW1CS	0	**Malformed TLP Status**
17	RW1CS	RW1CS	0	**Receiver Overflow Status (Optional)**
16	RW1CS	RW1CS	0	**Unexpected Completion Status**
15	RW1CS	RW1CS	0	**Completer Abort Status (Optional)**
14	RW1CS	RW1CS	0	**Completion Timeout Status**
13	RW1CS	RW1CS	0	**Flow Control Protocol Error Status (Optional)**
12	RW1CS	RW1CS	0	**Poisoned TLP Status**
11:6	RO	RO	0	**Reserved**
5	RO	RO	0	**Surprise Down Error Status**
4	RW1CS	RW1CS	0	**Data Link Protocol Error Status**
3:1	RO	RO	0	**Reserved**
0	RO	RWS	0	**Undefined**

Offset 1_0Bh – 1_08h: PCI Express – Uncorrectable Error Mask

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:21	RO	RO	0	**Reserved**
20	RWS	RWS	0	**Unsupported Request Error Mask**
19	RWS	RWS	0	**ECRC Error Mask (Optional)**
18	RWS	RWS	0	**Malformed TLP Mask**
17	RWS	RWS	0	**Receiver Overflow Mask (Optional)**
16	RWS	RWS	0	**Unexpected Completion Mask**
15	RWS	RWS	0	**Completer Abort Mask (Optional)**
14	RWS	RWS	0	**Completion Timeout Mask**
13	RWS	RWS	0	**Flow Control Protocol Error Mask (Optional)**
12	RWS	RWS	0	**Poisoned TLP Mask**
11:6	RO	RO	0	**Reserved**
5	RWS	RWS	1b	**Surprise Down Error Mask**
4	RWS	RWS	1b	**Data Link Protocol Error Mask**
3:1	RO	RO	0	**Reserved**
0	RO	RWS	0	**Undefined**

Offset 1_0Fh – 1_0Ch: PCI Express – Uncorrectable Error Severity

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:21	RO	RO	0	**Reserved**
20	RWS	RWS	0	**Unsupported Request Error Severity**
19	RWS	RWS	0	**ECRC Error Severity (Optional)**
18	RWS	RWS	1b	**Malformed TLP Severity**
17	RWS	RWS	1b	**Receiver Overflow Error Severity (Optional)**
16	RWS	RWS	0	**Unexpected Completion Error Severity**
15	RWS	RWS	0	**Completer Abort Error Severity (Optional)**
14	RWS	RWS	0	**Completion Timeout Error Severity**
13	RWS	RWS	1b	**Flow Control Protocol Error Severity (Optional)**
12	RWS	RWS	0	**Poisoned TLP Severity**
11:6	RO	RO	0	**Reserved**
5	RWS	RWS	1b	**Surprise Down Error Severity**
4	RWS	RWS	1b	**Data Link Protocol Error Severity**
3:1	RO	RO	0	**Reserved**
0	RO	RWS	1b	**Undefined**

Offset 1_13h – 1_10h: PCI Express – Correctable Error Status

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:14	RO	RO	0	**Reserved**
13	RW1CS	RW1CS	0	**Advisory Non-Fatal Error Status**
12	RW1CS	RW1CS	0	**Replay Timer Timeout Status**
11:9	RO	RO	0	**Reserved**
8	RW1CS	RW1CS	0	**REPLAY_NUM Rollover Status**
7	RW1CS	RW1CS	0	**Bad DLLP Status**
6	RW1CS	RW1CS	0	**Bad TLP Status**
5:1	RO	RO	0	**Reserved**
0	RW1CS	RW1CS	0	**Receiver Error Status (Optional)**

Offset 1_17h – 1_14h: PCI Express – Correctable Error Mask

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:14	RO	RO	0	**Reserved**
13	RW	RW	1b	**Advisory Non-Fatal Error Mask**
12	RWS	RWS	0	**Replay Timer Timeout Mask**
11:9	RO	RO	0	**Reserved**
8	RWS	RWS	0	**REPLAY_NUM Rollover Mask**
7	RWS	RWS	0	**Bad DLLP Mask**
6	RWS	RWS	0	**Bad TLP Mask**
5:1	RO	RO	0	**Reserved**
0	RWS	RWS	0	**Receiver Error Mask (Optional)**

Offset 1_1Bh – 1_18h: PCI Express – Advanced Error Capability and Control

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:9	RO	RO	0	**Reserved**
8	RWS	RWS	0	**ECRC Check Enable**
7	RW	RO	1b	**ECRC Check Capable**
6	RWS	RWS	0	**ECRC Generation Enable**
5	RW	RO	1b	**ECRC Generation Capable**
4:0	ROS	ROS	0	**First Error Pointer**

Offset 1_2Bh – 1_1Ch: PCI Express – Header Log Registers

Bit	Attribute		Default	Description
	SMBus	PCIe		
127:0	ROS	ROS	0	**Header of TLP Associated with Error**

Offset 1_33h – 1_30h: Device Serial Number Enhanced Capability

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:20	RO	RO	0	**Device Serial Number Next Pointer (DSNNXPTR)**
19:16	RO	RO	01h	**Device Serial Number Capability Version (DSNCAP_VER)**
15:0	RO	RO	0003h	**Extended Capability ID**

Offset 1_37h – 1_34h: Device Serial Number [31:0] - Lower

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:16	RE	RE	0	**DSNR1_LO**
15:0	RE	RE	0	**DSNR0_LO**

Offset 1_3Bh – 1_38h: Device Serial Number [63:32] - Upper

Bit	Attribute		Default	Description
	SMBus	PCIe		
31:16	RE	RE	0	**DSNR1_UP**
15:0	RE	RE	1106h	**DSNR0_UP**

Control and Status Register

Ethernet Node Address Register (Offset 00-05h)

Offset 05h – 00h: Ethernet Node Address (PAR5 – PAR0)

Bit	Attribute	Default	Description
47:0	RWE	0	**PAR5 – PAR0 Ethernet Node Address**. Ethernet node ID for unicast address filtering loaded from EEPROM at power up. PAR5~PAR0 is Ethernet node ID[47:0], loaded from EEPROM at suspend power on. PCI reset sequence is done or software driven reload process, also can be updated by software. The Node ID Registers are used to do unicast packets physical address filtering.

Receive Control Register (Offset 06h)

Offset 06h: Receive Control Register (RCR)

The RCR is reset by H_RESET and S_RESET.

Bit	Attribute	Default	Description
7	RW	0	**AS**. Accept symbol error packet with good CRC 0: Disable 0: Enable
6	RW	0	**AP**. Accept packet through perfect-filtering. Leave the receive type status to RD write-back status 0: Disable 0: Enable
5	RW	0	**AL**. Accept long packet, 1518 / 1522 (if contain TAG) 0: Disable 0: Enable
4	RW	0	**PROM**. Promiscuous Mode. Accept all physical address packets 0: Disable 0: Enable
3	RW	0	**AB**. Accept Broadcast packet 0: Disable 0: Enable
2	RW	0	**AM**. Accept Multicast packet 0: Disable 0: Enable
1	RW	0	**AR**. Accept Runt packet 0: Disable 0: Enable
0	RW	0	**SEP**. Accept addressed packet with CRC error. 0: Disable 0: Enable

AP=1: accept CRC ok packet as A-CAM hit. Not stock by AB/AM/PROM/DISAU setting

AP=0: packet acceptation depends on AB/AM/PROM/DISAU setting.

Offset 07h: Transmit Control Register (TCR)

The TCR is reset by H_RESET and S_RESET.

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	0	**COLTMC[1:0]** Collision retry control before aborting current transmission. 00: Normal 16-times 01: 2 Sets, 32-times 10: 3 Sets, 48-times 11: Retry forever
1:0	RW	0	**LB[1:0]**. Internal/external loopback control 00: Normal 01: MAC Internal 10: External 11: Reserved

Notes:
1. The TCR is reset by H_RESET and S_RESET.
2: Loopback control will be divided into MII and GMII mode.

Offset 08h: Global Command Register (CR0.s)

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW1	0	**TXON**. Transmit process enable. Check the relationship with TD RUN bits. 0: Disable 1: Enable
2	RW1	0	**RXON**. Receive process enable. Check the relationship with RD RUN bits 0: Disable 1: Enable
1	RW1	0	**STOP**. STOP NIC, reset STRT, default =1, set while S_RST, H_RST 0: Disable 1: Enable
0	RW1	0	**STRT**. START NIC, reset while STOP or S_RST, H_RST Before turning on TXON/RXON, STRT must be enabled.

Note: STOP/STRT/TXON/RXON refer to TX/RX shut down routine AP note

Offset 09h: Global Command Register 1 (CR1.s)

Bit	Attribute	Default	Description
7	RW1C	0	**SFRST**. Software reset. Self-Cleared after internal logic reaching safe states.
6	RW1	0	**TM1EN**. Enable periodic Software Timer counting
5	RW1	0	**TM0EN**. Enable single-shot Software Timer counting
4:3	RO	0	**Reserved**
2	RW1	0	**MDISAB**. Disable accept broadcast packet when AM = 1
1	RO	1b	**Reserved** (Do not program)
0	RW1	0	**DISAU**. Unicast Reception Disable

Note: STOP/STRT/TXON/RXON refer to TX/RX shut down routine AP note

Offset 0Ah: Global Command Register 2 (CR2.s)

Bit	Attribute	Default	Description
7	RW1	0	**XONEN**. IEEE 802.3x, XON/XOFF mode enable 0: Never transmit XON frame always. 1: NIC will transmit XON frame (Pause Timer = 16'h0000) as local Tx Pause Frame expired.
6	RW1	0	**FDXTFCEN**. Full-duplex flow control TX enabled.
5	RW1	0	**FDXRFCEN**: Full-duplex flow control RX enabled
4	RW1	0	**HDXFCEN**. Half-duplex flow control enabled.
3:2	RW	0	**XHITH[1:0]**. Transmit XON frame high threshold XHITH1 XHITH0 0 0 24 0 1 32 1 0 48 1 1 64
1:0	RW	11b	**XLITH[1:0]**. Transmit pause frame Low threshold XLTH1 XLTH0 0 0 4 0 1 8 1 0 16 1 1 24

Offset 0Bh: Global Command Register 3 (CR3.s)

Bit	Attribute	Default	Description
7	RW1	0	**GSPRST**. Software generated force suspend reset for diagnosis purpose only. – issue SUSPRSTZ – issue PHYRSTZ – restart GTXC_SRC – NOT reset PLL – NOT get new strapping value
6:3	RO	0	**Reserved**
2	RW1	0	**INTPCTL**. Enable interrupt pending hold-off timer control 0: No timer based interrupt pending control 1: Enable interrupt hold-off pending control
1	RW1	0	**GintMsk1**. Global Interrupt Mask 1. Disable INTA# generation from all ISR bits
0	RW1	0	**GintMsk0**. Software controls multiple level Interrupt Mask 0. Disable INTA# generation from multi-level ISR bits defined in ISR_CTL PMSK[1:0]

Offset 0Fh – 0Ch: Command Register Clear Port

Bit	Attribute	Default	Description
31:0	RW0	0	**CR3.c, CR2.c, CR1.c, CR0.c** Write "1" to clear the indexed register bit in command set port and clear.

Offset 17h ~ 10h: MultiCast Hashing Table Register

Offset 0x17h ~0x10h are shared with address recognition logic. MAR7~MAR0 are put on page 0 for 64-bit hashing table of multicast filtering. The mask bits of Address perfect filtering CAM and VLAN ID CAM are put on page 1. The data of Address perfect filtering CAM and VLAN ID CAM are put on page 2. The page definition is controlled by offset 69[7:6], PS[1:0]. (PS1, PS0) = (0,0) is for MAR port, while (PS1, PS0)=(0,1) is for CAM Mask port and (PS1, PS0)=(1,0) is for CAM Data port.

In Summary,

- Support 64-bit multicast hashing enable MAR0~MAR7
- Support 64-bit address perfect filtering enable masks, and 64-bit VLAN ID perfect filtering enable masks
  A_CAM data: {CAM5,CAM4,CAM3,CAM2,CAM1,CAM0}
  V_CAM data: {CAM1,CAM0}
  A_CAM mask: {CAM7,CAM6,CAM5,CAM4,CAM3,CAM2,CAM1,CAM0}
  V_CAM mask: {CAM7,CAM6,CAM5,CAM4,CAM3,CAM2,CAM1,CAM0}

Bit	Attribute	Default	Description
63:0	RW	0	**MAR7~MAR0. 64-bit hashing table** The registers are used to do multicast packets address filtering.

Offset 17h – 10h: PCAM/VCAM Data and Mask Register

Bit	Attribute	Default	Description
63:0	RW	0	**CAM7~CAM0. 64-bit hashing table** Accessed by CAM embedded Control and Data Port.

Offset 1Bh – 18h: Tx/Rx Descriptor Base Address High Register

Bit	Attribute	Default	Description
31:0	RW	0	**DescBaseHi[63:32].** Tx/Rx Descriptor High Address.

Offset 1Dh – 1Ch: Tx/Rx Common Data Buffer Base Address High Register

R/W if 64-bit addressing, else read as 16'h0 always, in data buffer case only support up to 48-bit memory space range, address bits on 63-48 defined different memory range. In 64-bit addressing, all descriptor linked data buffers use the same common high 16-bit addressing base.

Bit	Attribute	Default	Description
15:0	RW	0	**DataBufBaseHi[63:48].** Tx/Rx Descriptor Linked Data Buffer High Address.

Offset 21h – 20h: Interrupt Control 0, 1 Register

Interrupt Control by Software using hardware timer, the pending control only mask the interrupt source from UDPINT, PRXI, PTX0~3I.

When SC turn on the interrupt pending hold off control by set INTPCTL=1, Before SC try to write clear the ISR bits, SC will set INT_Pending to instruct HC to reload INTHOTMR, and hardware begin to count down and enable interrupt pending control, when the count down process reach zero, the INT_pending bit will be cleared to "0" by HC. HC also supports multiple INT_Pending control to extend the pending window. Any time Software can release the INT pending control by clear INTPCTL bit in CR2[19]. All control except UDPINT,in ISR_CTL are enabled by INTPCTL bit = 1.

<table>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Description</th></tr>
<tr><td>15</td><td>R0W</td><td>0</td><td>UDPINT.s. User define interrupt set port. Always read as 0.</td></tr>
<tr><td>14</td><td>RW</td><td>0</td><td>TSUPP_DIS. Disable Tx interrupt suppression feature.</td></tr>
<tr><td>13</td><td>RW</td><td>0</td><td>RSUPP_DIS. Disable Rx interrupt suppression feature.</td></tr>
<tr><td>12:11</td><td>RW</td><td>00b</td><td>PMSK[1:0]. Interrupt masks selection bits for multiple levels interrupt control
00: Mask Layer-0 Events
01: Mask Layer-1 Events
10: Mask All Interrupt Events
11: Mask All Interrupt Events</td></tr>
<tr><td>10</td><td>ROC</td><td>0</td><td>INT_Pending. Hardware hold-off Interrupt Pending status.</td></tr>
<tr><td>9</td><td>RW</td><td>0</td><td>HC_RELOAD. In this mode, INTHOTMR is reloaded when HFLD bit in ISR2 is set.</td></tr>
<tr><td>8</td><td>R0W</td><td>0</td><td>SC_RELOAD. INTPCTL=1 and HC_RELOAD=0; INTHOTMR is reloaded when this bit is write A "1". Always read as "0".</td></tr>
<tr><td>7:0</td><td>RW</td><td>0</td><td>
<table>
<tr><th colspan="3">Page selector {PS1, PS0}</th></tr>
<tr><td>0 0</td><td>0 1</td><td>1 0</td></tr>
<tr><td>INTHOTMR</td><td>TSUPPTHR</td><td>RSPPTHR</td></tr>
</table>
INTHOTMR. Counter values to prevent interrupt assertion for a programmed time period. When ISR is written cleared, the internal interrupt hold off timer is loaded with this value. It begins to count down when INTPCTL bit is set, once it reach "0" the interrupt will be enabled again. This feature a timer based adaptive interrupt scheme. Resolution=20 us. Enable when INTPCTL=1
(Resolution:
EEFAST = 1, TimeOut = 256ns/ 320ns (31M / 25M)
EEFAST = 0, TimeOut = 16.38us/ 20.48us (31M / 25M)
TSUPPTHR. Tx interrupt-suppression threshold register. While tx int-suppr enabled (TSUPPD=0), the served tx packet will be counted one by one. Once the served number equals to this threshold register, high priority interrupt (PPTXI) will be set.
RSUPPTHR. Rx interrupt-suppression threshold register. While rx int-supp enabled (RSUPPD=0), the served RD will be counted one by one. Once the served RD number equals to this threshold register, high priority interrupt (PPRXI) will be set.</td></tr>
</table>

Notes:
1. GintMsk0 is in CR3[0], GintMsk1=CR3[1], INTPCTL in CR3[2].
2. Clear INTPCTL will release hold-off pending control immediately.
3. Multiple level Interrupt pending control is controlled by PMSK[1:0].

Layer-0	ISR0: PTXnI, PRXI,PTXI. ISR1: FLONI. ISR2: UDPI,PWEI ISR3: ISRn
Layer-1	Layer-0 + ISR0: PPRXI, PPTXI.
Layer-2	All
Layer-3	All

Offset 22h: Transmit Host Error Status Register (TXE_SR)

These error statuses will cause TDCSR.Dead set and the "OR" operation of these statuses is reported on ISR3 TDSTLI for stall condition reporting.

Bit	Attribute	Default	Description
7:4	R0	0	**ZeroBit**.
3	RW0S	0	**TFDBS**. Transmit FIFO DMA bus error
2	RW0S	0	**TDWBS**. TD write back host bus error
1	RW0S	0	**TDRBS**. TD descriptor fetch host bus error
0	RW0S	0	**TDSTR**. TD Structure Error (1) TD link structure error. (2) Valid buffer segment (CMDZ) with zero buffer length.

Offset 23h: Receive Host Error Status Register (RXE_SR)

These error statuses will cause RDCSR.Dead being set and the "OR" operation of these statuses is reported on ISR3 RDSTLI for stall condition reporting.

Bit	Attribute	Default	Description
7:4	R0	0	**ZeroBit**.
3	RW0S	0	**RFDBS**. Rx FIFO DMA experience Host bus error. Write 1: clear the bit Write 0: remain unchanged.
2	RW0S	0	**RDWBS**. RD write back host bus error Write 1: clear the bit Write 0: remain unchanged.
1	RW0S	0	**RDRBS**. RD Fetch host bus error. Write 1: clear the bit Write 0: remain unchanged.
0	RW0S	0	**RDSTR**. RD Structure Error. Write 1: clear the bit Write 0: remain unchanged. (1) Valid RD with linked buffer size zero.

Interrupt Status Registers (Offset 24 – 27h)

Offset 27h ~ 24h are the interrupt status registers. The interrupt event source bits are arranged to meet the Interrupt service hierarchy to maintain an efficient searching and programming methodology.

Offset 24h: Interrupt Status Register 0 (ISR0)

ISR0 shows service complete events of transmission and reception. PTXn, PRXI show a packet based event reporting. Besides, the IMR control the INT reporting, these 5 interrupt source will be further masked to avoid new normal INT generation by any mechanism implemented in interrupt control logics.

Bit	Attribute	Default	Description
7:4	RW0S	0	**PTX[3:0]I**. Transmit service Complete status in TD queue #3,2,1,0. Write 1: clear the bit Write 0: remain unchanged
3	ROS	0	**PTXI**. Combination results of PTXnI, Read Only
2	RW0S	0	**PRXI**. Receive Service complete Write 1: clear the bit Write 0: remain unchanged
1	RW0S	0	**PPTXI**. High priority transmit interrupt Service Request. PTXn will be also set. Write 1: clear the bit Write 0: remain unchanged
0	RW0S	0	**PPRXI**. High priority receive interrupt Service Request. PRXI will be also set. Write 1: clear the bit Write 0: remain unchanged

Software Service Policy.

1. Check PRXI and PTXI first in normal events service.
2. If interrupt pending control is running, the interrupt is sourced from PPTXI or PPRXI, SC need to clear the interrupt source at both P/PP levels.
3. Software can simply use 0x0Fh in IMR setting

Offset 25h: Interrupt Status Register 1 (ISR1)

Bit	Attribute	Default	Description
7	RW0S	0	**SRCI**. Port Status Change Write 1: clear the bit Write 0: remain unchanged
6	RW0S	0	**LSTPEI**. RD List is using up warning. Write 1: clear the bit Write 0: remain unchanged LSTPEI is available only while TX flow control enabled.
5	RW0S	0	**LSTEI**. Receive Descriptor (RD) is used up Write 1: clear the bit Write 0: remain unchanged
4	RW0S	0	**OVFI**. Receive FIFO overflow. Some receive packets might be lost in this case Write 1: clear the bit Write 0: remain unchanged
3	RW0S	0	**FLONI**. Receive flow control mechanism turn on status as a notification to driver Write 1: clear the bit Write 0: remain unchanged
2	RW0S	0	**RACEI**. Receive FIFO Packet List Queue overflow Write 1: clear the bit Write 0: remain unchanged
1	RW	0	**TDWB1I**
0	RW	0	**TDWB0I**

Offset 26h: Interrupt Status Register 2 (ISR2)

Bit	Attribute	Default	Description
7	R0W1	0	**HFLD**. Write 1 to enable hold off timer reload. Read as 0 always
6	RW0S	0	**UDPI**. User defined, software driven interrupt for diagnosis. Write 1: clear the bit Write 0: remain unchanged
5	RW0S	0	**MIBFI**. MIB counter near full. Warning, Write 1: clear the bit Write 0: remain unchanged
4	RW0S	0	**SHDNII**. Software shut down complete. Write 1: clear the bit Write 0: remain unchanged
3	RW0S	0	**PHYI**. While PHYINTEN is enabled, this bit shows phy interrupt event occurred.
2	RO	0	**PWEI**. Wake up power events reporting status for test purpose
1	RW0S	0	**TMR1I**. Programmable software Timer 1 expired interrupt status. Write 1: clear the bit Write 0: remain unchanged
0	RW0S	0	**TMR0I**. Programmable software Timer 0 expired interrupt status. Write 1: clear the bit Write 0: remain unchanged

Note: HFLD is for special purpose. IMR23 is reserved.

Offset 27h: Interrupt Status Register 3 (ISR3)

ISR3 shows source and TX/RX DMA error. This register is read only. To clear the interrupt, it is necessary to write clearing related source.

Bit	Attribute	Default	Description
7:4	RO	0	**ISRn**. Interrupt Source Indication.
3:2	RO	0	**Reserved**
1	RO	0	**TXSTLI**. Transmission DMA stall in TXE_SR.
0	RO	0	**RXSTLI**. Receive DMA Stall in RXE_SR.

Note: Normally, there is no need to turn on the mask of IMR31~IMR26.

Interrupt Enable Register (Mask) (Offset 28h – 2Bh)

Interrupt enable of ISR0 ~ ISR3. The interrupt signaling INTA# is driven while |(ISRn & IMRn)= interruptTriggered, (n=0 to 31), since INTA# is for shared bus and is a open drain pin, output enable of INTA_ = interruptTriggered, INTA_ = !(interruptTriggered).
→ MIMR0 → IMR2, MIMR1 → IMR2.

Offset 2B-28h: Interrupt Enable Register (IMR3 - IMR0)

Bit	Attribute	Default	Description
31:0	RW	0	**IMRn**. Interrupt Source Enable Control.

Tx Descriptor Control Status Register (Offset 30 – 31h, Offset 34 – 35h)

Offset 30h: Tx Descriptor Control Status Registers Set (TDCSR0.s)

Bit	Attribute	Default	Description
7	RWS	0	**DEAD1**. Indicate TD queue #1 encounters error conditions. (Set by HW / Reset by SW)
6	RWC	0	**WAK1**. Wake up TD queue #1 to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
5	RU	0	**ACT1**. Indicate the end of TD queue #1 has not been reached when processing descriptors. (Set and Reset by HW)
4	RW	0	**RUN1**. Enable TD queue #1 to operation. (Set and Reset by SW)
3	RWS	0	**DEAD0**. Indicate TD queue #0 encounters error conditions. (Set by HW / Reset by SW)
2	RWC	0	**WAK0**. Wake up TD queue #0 to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
1	RU	0	**ACT0**. Indicate the end of TD queue #0 has not been reached when processing descriptors. (Set and Reset by HW)
0	RW	0	**RUN0**. Enable TD queue #0 to operate. (Set and Reset by SW)

Offset 31h: Tx Descriptor Control Status Registers Set (TDCSR1.s)

Bit	Attribute	Default	Description
7	RWS	0	**DEAD3**. Indicate TD queue #3 encounters error conditions. (Set by HW / Reset by SW)
6	RWC	0	**WAK3**. Wake up TD queue #3 to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
5	RU	0	**ACT3**. Indicate the end of TD queue #3 has not been reached when processing descriptors. (Set and Reset by HW)
4	RW	0	**RUN3**. Enable TD queue #3 to operation. (Set and Reset by SW)
3	RWS	0	**DEAD2**. Indicate TD queue #2 encounters error conditions. (Set by HW / Reset by SW)
2	RWC	0	**WAK2**. Wake up TD queue #2 to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
1	RU	0	**ACT2**. Indicate the end of TD queue #2 has not been reached when processing descriptors. (Set and Reset by HW)
0	RW	0	**RUN2**. Enable TD queue #2 to operate.(Set and Reset by SW)

Offset 35h ~ 34h: Tx Descriptor Control Status Register Clear (TDCSR0.c)

Write 1 will clear related TDCSR bit and won't take effect if write 0 on these bits.
Reading offset 30h or 34h will return the same values.

Bit	Attribute	Default	Description
15:8	RW0	0	Bit definitions are the same as TDCSR1.s (offset 31h).
7:0	RW0	0	Bit definitions are the same as TDCSR0.s (offset 30h).

Rx Descriptor Control Status Register 0 Set / Clear (Offset 32 – 33h, Offset 36 – 37h)

Write 1 will set RDCSR bits and will not take effect if write 0.

Offset 33h – 32h: Rx Descriptor Control Register 0 Set (RDCSR.s)

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3	RWS	0	**DEAD**. Indicate current queue encounters error conditions. (Set by HW / Reset by SW)
2	RWC	0	**WAK**. Wake RD queue to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
1	RU	0	**ACT**. Indicate RD list end has not been reached when processing descriptors. (Set and Reset by HW) 0: RX channel inactive. NIC won't fetch RD automatically until WAK command issued. 1: RX channel active. NIC will auto fetch next RD if needed.
0	RW	0	**RUN**. Enable queues to operate. (Set and Reset by SW)

Offset 37h – 36h: Rx Descriptor Control Register 0 Clear (RDCSR.c)

Reading offset 32h or 36h will return the same values.

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW0	0	Bit definitions are the same as RDCSR0.s (offset 32h)

Rx Descriptor Base Address Low Register (Offset 38 – 3Bh)

Offset 3Bh ~ 38h: Descriptor Base Address Low (RxDsBase.Lo)

Bit	Attribute	Default	Description
31:6	RWU	0	**RxDsBase.Lo[31:6]:** RD Base Address Low
5:0	R0	0	R/W as 0 always. For descriptor alignment issue

Current Rx Descriptor Index Register (Offset 3C – 3Dh)

Offset 3Dh – 3Ch: Current Rx Descriptor Index Register (RDINDX)

Current Receive Descriptor List Index maintained by HC in ring structure.

Bit	Attribute	Default	Description
15:0	RU	0	**RdIndex**. Current indexed RD, will cross top while reach the RDCSIZE defined in offset 50h.

Pending Timer for Tx Queue/Rx Queue Empty Interrupt (Offset 3E – 3Fh)

Offset 3Fh – 3Eh: Pending Timer For Tx Queue/Rx Queue Empty Interrupt (TQETMR, RQETMR)

The unbalanced bandwidth between host side (PCI) and media side will induce the internal TXFIFO/RXFIFO to reach empty state and issue interrupt event frequently. To avoid this, 2 dedicated timers are provided to suspend this interrupt caused of TXFIFO/RXFIFO empty state respectively.

Bit	Attribute	Default	Description
15:14	RW	0	**RQETMS[1:0]**. Timer resolution selection 00: 1 us 01: 4 us 10: 16 us 11: 64 us
13:8	RW	0	**RQETMR: Pending Time Count**
7:6	RW	0	**TQETMS[1:0]**. Timer resolution selection 00: 1 us 01: 4 us 10: 16 us 11: 64 us
5:0	RW	0	**TQETMR**. Pending Time Count

Tx Descriptor 0 Base Address Low Register (Offset 40 – 4Fh)

Offset 43h – 40h: Tx Descriptor 0 Base Address Low Register (TdBase0.Lo)

Bit	Attribute	Default	Description
31:6	RW	0	**TdBase0Lo[31:6]**. TD #0 Base Address Low
5:0	R0	0	R/W as 0 always. For descriptor alignment issue.

Offset 47h – 44h: Tx Descriptor 1 Base Address Low Register (TdBase1.Lo)

Bit	Attribute	Default	Description
31:6	RW	0	**TdBase1Lo[31:6]**. TD #1 Base Address Low
5:0	R0	0	R/W as 0 always. For descriptor alignment issue.

Offset 4Bh – 48h: Tx Descriptor 2 Base Address Low Register (TdBase2.Lo)

Bit	Attribute	Default	Description
31:6	RW	0	**TdBase2Lo[31:6]**. TD #2 Base Address Low
5:0	R0	0	R/W as 0 always. For descriptor alignment issue.

Offset 4Fh – 4Ch: Tx Descriptor 3 Base Address Low Register (TdBase3.Lo)

Bit	Attribute	Default	Description
31:6	RW	0	**TdBase3Lo[31:6]**. TD #3 Base Address Low
5:0	R0	0	R/W as 0 always. For descriptor alignment issue.

Descriptor Size Register (Offset 50 – 53h)

Offset 53h – 50h: Descriptor Size Register (TDCSIZE, RDCSIZE)

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved.**
27:16	RW	0	**TDCSIZE[11:0]**. Tx Descriptor list length in each TD queue
15:0	RW	0	**RDCSIZE**. Tx Descriptor RD list length.

Current Tx Descriptor Index Register (Offset 54 – 5Bh)

Offset 57h – 54h: Current Tx Descriptor Index. 0, 1 (TdIndxn)

Current Transmit Descriptor List Index maintained by HC in ring structure.

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved.** Read as 0 always
27:16	RU	0	**TdIndex1**. Current indexed TD in queue #1. Cross top while reaching the TDCSIZE defined in offset 52h.
15:12	RO	0	**Reserved**. Read as 0 always
11:0	RU	0	**TdIndex0**. Current indexed TD in queue #0. Cross top while reaching the TDCSIZE defined in offset 52h.

Note:
Maximum 4096 index number for TD0~TD3, to define the list top
For debugging purpose, these indices can be set manually when RUNX is 0 (Queue is temporarily blocked from normal operation).
TDIDX[7:0]: indicate current TD index in TD ring.

1. Self reset to 0 while program TDBaseLo.
2. Self return to 0 while cross TDCSIZE.
3. Auto-increase as TD ring advanced.
4. SW could program TDIDX while RUN = 0

Offset 5Bh – 58h: Current Tx Descriptor Index 2, 3 (TdIndxn)

Current Transmit Descriptor List Index maintained by HC in ring structure.

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved.** Read as 0 always
27:16	RU	0	**TdIndex3**. Current indexed TD in queue #3. Cross top while reaching the TDCSIZE defined in offset 52h.
15:12	RO	0	**Reserved.** Read as 0 always
11:0	RU	0	**TdIndex2**. Current indexed TD in queue #2. Cross top while reaching the TDCSIZE defined in offset 52h.

Note:
Maximum 4096 index number for TD0~TD3, to define the list top
For debugging purpose, these indices can be set manually when RUNX is 0 (Queue is temporarily blocked from normal operation).
TDIDX[7:0]: indicate current TD index in TD ring.

1. Self reset to 0 while program TDBaseLo.
2. Self return to 0 while cross TDCSIZE.
3. Auto-increase as TD ring advanced.
4. SW could program TDIDX while RUN = 0.

Tx Programmable Pause Frame Timer Register (Offset 5C – 5Dh)

Offset 5Dh – 5Ch: Tx Programmable Pause Frame Timer (TXPUTM)

Bit	Attribute	Default	Description
15:0	RW	0	**TXPUTM[15:0]**. Software programmed pause frame timer in transmitted pause frame

Flow Control Rx Descriptor Residue Count Register (Offset 5E – 5Fh)

Offset 5Fh – 5Eh: Flow Control Rx Descriptor Residue Count (RBRDU)

Receive descriptor list usage control registers for flow control busy condition in system buffer side. Negotiated between Software and HC.

Bit	Attribute	Default	Description
15:0	RW	0	**RBRDU**. Rx Descriptor buffer residue counts. RXON disabled: update Rx buffer counts with Value RXON enabled: add Rx buffer counts with Value

Offset 67h – 60h: Reserved

CAM Control Register (Offset 68 – 69h)

Offset 68h: CAM Address Register (CAMADR)

Bit	Attribute	Default	Description
7	RW	0	**CAMEN.** Enable CAM Read/Write command.
6	RW	0	**CA6.** A-CAM/V-CAM Address Bit 6. A-CAM/V-CAM selection bit A-CAM while CA6 = 0 V-CAM while CA6 = 1.
5:0	RW	0	**CA[5:0].** A-CAM/V-CAM Address

Offset 69h: CAM Command Register (CAMCR)

Bit	Attribute	Default	Description
7:6	RW	0	**PS[1:0].** Page Select. Register Page Select of MAR/VCAM/PCAM. Offset 10h-17h / Offset 20h / Offset C0h 00: MAR port / INTHOTMR / ptn (0,1,2,3) 01: CAM Mask Port / TSUPPTHR / ptn (4,5,6,7) 10: CAM Data Port / RSUPPTHR / ptn (0,1,2,3) 11: MAR port / INTHOTMR / ptn (4,5,6,7)
5	RW	0	**AITRPKT**. Partition part of Address-CAM space for interesting packets filtering. 0: No Interesting packet segment defined. 1: With Interesting packet segment defined.
4	RW	0	**AITR16**. Interesting packet segment in A-CAM size option. Available only when bit 5 is enabled (set to 1) 0: 8 entries (cam_add 56 ~ 63) 1: 16 entries (cam_add 48 ~ 63)
3	RWC	0	**CAMRD**. CAM read command, auto cleared. Work only while CAMEN is enabled.
2	RWC	0	**CAMWR**. CAM write command, auto cleared. Work only while CAMEN is enabled.
1:0	RO	0	**Reserved**

Offset 6Bh-6Ah: Reserved

MII Management Port Control Status Registers (Offset 6Ch – 73h)

Offset 6Ch: MII Management Port Configuration Register (MIICFG)

MIICFG should be located at suspend domain.

Bit	Attribute	Default	Description
7:6	RW	0	**MPO1, MPO0x**. MII management polling interval, time unit = MDC clock cycle. MPO1 MPO0 MDCs 0 0 1024 0 1 512 1 0 128 1 1 64
5	RW	0	**MFDC**. Accelerate MDC Speed 0: MDC = normal 1: MDC = 4X accelerating
4	RO	1b	**J_FRCDPLX**. Force full duplex mode.
3	RO	0	**J_ANEGDIS**. Force auto-negotiation disable.
2	RO	1b	**J_MASTER**. Force master mode.
1	RO	1b	**J_MODE100**. Force MII 100 mode.
0	RO	0	**J_MODE1000**. Force MII 1000 mode.

Offset 6Dh: MII Management Port Status Register (MIISR)

Bit	Attribute	Default	Description
7	RW	0	**MIIDL**. Indicate not at the Software/Timer polling cycle
6:0	RO	0	**Reserved**

Offset 6Eh: PHY Status Register 0 (PHYSR0)

Bit	Attribute	Default	Description
7	RO	0	**PHYRST**. Show the PHY.Reg0.Bit15, RESET while PHYRST=1, all other bits are junk
6	RO	0	**LINKGD**. Show PHY.Reg1.Bit2, Link Status
5	RO	0	**Reserved**
4	RO	1b	**FDPX**. Full duplex mode, Pri-Res-Result. Priority Resolution Result.
3	RO	1b	**SPDG**. PHY in Giga mode, Pri-Res-Result. Priority Resolution Result.
2	RO	0	**SPD10**. PHY in 10M mode, Pri-Res-Result. Priority Resolution Result.
1	RO	0	**RXFLC**. Rx flow control capability. Pri-Res-Result. Priority Resolution Result.
0	RO	0	**TXFLC**. Tx flow control capability. Pri-Res-Result. Priority Resolution Result.

Offset 6Fh: Reserved

Offset 70h: MII Management Command Register (MII_CR)

Bit	Attribute	Default	Description
7	RW	0	**MAUTO**. MII management port auto polling enable. MIICR has no effect while this bit is 1.
6	RWC	0	**RCMD**. MII management port embedded read command. Self-cleared while reading is completed. Available only while MAUTO=0 and MDPM=0.
5	RWC	0	**WCMD**. MII management port embedded write command. Reset while reading is completed and PHY status is stored in offset 72h.
4	RW	0	**MDPM**. MII management port direct programming enable. Reset while programming is completed.
3	RW	0	**MOUT**. MDIO pin output enable control in Direct Programming mode.
2	RW	0	**MDO**. MDIO pin output data in Direct Programming mode
1	RW	0	**MDI**. MDIO pin input data in Direct Programming mode.
0	RW	0	**MDC**. MDC pin output data in Direct Programming mode.

Note:
MII Embedded Programming
Offset 70[5] (WCMD):
Write the offset address to Offset 71.
Write the programmed value to Offset 72/Offset 73
Program MIICR.WCMD.
Wait MIICR.WCMD cleared. The programming sequences are completed.

Offset 70[6] (RCMD):
Write the offset address to Offset 71.
Program MIICR.RCMD.
Wait MIICR.RCMD cleared. The reading sequences are completed.
Read Offset 72/Offset 73 to get the value.

Offset 71h: MII Embedded Read/Write Address Port Register (MII_ADR)

FXMODE was moved to CHIPGCR (Offset 9F)

Bit	Attribute	Default	Description
7	RWC	0	**SWMPL.** Initiate the priority resolution process. Self-cleared while all cycles are completed.
6:5	RO	0	**Reserved**
4:0	RW	0	**MAD[4:0].** Target PHY Map register address for embedded read write process. While MIIPDIAG is enabled, MAD[1:0] are used for Priority Resolution Table Checking. MAD1: PHYRST MAD0: LINKSTS

Offset 73h – 72h: MII Embedded Read/Write Data Port Register (MII_DAT)

Access method.

Bit	Attribute	Default	Description
15:0	RW	0	**MII_DATA.** MII PHY Management embedded Read/Write data port. While MIIPDIAG is enabled, this port is used for Priority Resolution Table Checking. 15: LD Asym Pause 7: LP Asym Pause 14: LD Pause 6: LP Pause 13: LD 1000 Full 5: LP 1000 Full 12: LD 1000 Half 4: LP 1000 Half 11: LD 100 Full 3: LP 100 Full 10: LD 100 Half 2: LP 100 Half 9: LD 10 Full 1: LP 10 Full 8: LD 10 Half 0: LP 10 Half

Software Timer Registers (Offset 74h – 77h)

Offset 75h – 74h: Software Single-shot Timer 0 Register (SFTMR0)

Operation:

a. Set resolution (GCR.TM0US) and program SFTMR0 register.
b. Set CR2.Timer0En=1.
c. SFTMR0 will be loaded and count down.
d. As timer expired, set timer0 interrupt (ISR2.TMR0I)
e. After write clear the ISR. TMR0I, SFTMR0 will be reloaded and count down again.
f. Clear CR2.Timer0EN will stop the behavior.

Bit	Attribute	Default	Description
15:0	RW	0	**SFTMR0**. Software programmable Timer with single shot. GCR.TM0US = 0 Resolution = 1.31ms GCR.TM0US = 1 Resolution = 1.28 us

Offset 77h – 76h: Software Periodic Timer 1 Register (SFTMR1)

Operation:

a. Set resolution (GCR.TM1US) and program SFTMR1 register.
b. Set CR2.Timer1En=1.
c. SFTMR1 will be loaded and count down.
d. As timer expired, set timer1 interrupt (ISR2.TMR1I)
e. SFTMR1 will be reloaded and count down again after timer-expired-interrupt is issued.
f. Clear CR2.Timer1EN will stop the behavior.

Bit	Attribute	Default	Description
15:0	RW	0	**SFTMR1.** Software programmable Timer with Periodic shot. GCR.TM1US = 0 Resolution = 1.31ms GCR.TM1US = 1 Resolution = 1.28 us

Chip Configuration Registers (Offset 78h – 7Fh)

Offset 78h: Chip Configuration Register A (CFG_A)

Configuration for Suspend Well function. Load from EEPROM at power up and can be updated by software.

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RWE	0	**LEDPCIVF.** Have all LEDs dark while PCI main power off.
5:4	RWE	01b	**PHYLEDS[1:0].** PHY LED function selection.
3	RWE	0	**PMHCTG.** Option to skip 802.1p TAG field while calculating the CRC value of incoming pattern-match packets. 0: TAG field is always skipped. 1: TAG field is included.
2	RWE	0	**PEXWAKE_OPT.** PCI Express Wake Option. 0: PME 1: Beacon
1	RWE	0	**ABSHDN.** Abnormal shut-down wake up function
0	RWE	0	**PACPI.** Pre_ACPI wake up function.

Offset 79h: Chip Configuration Register B (CFG_B)

Configuration for MAC function. Load from EEPROM at power up, can be updated by software.
Bit [7:6] are located at suspend domain.

Bit	Attribute	Default	Description
7	RWE	0	**GTCKOPT**. 0: GTXCLK will be exported while LinkDown 1: GTXCLK will not be exported while LinkDown GTXCLK behavior: Link on 10/100 BT:GTXCLK always be stopped. Link on 1000BT: (GTCKOPT==0) → always running (GTCKOPT==1) → Running while LinkOn, Stop while Linkdown.
6	RO	0	**Reserved**
5	RWE	0	**CRSEOPT.** Giga mode slot time option on receive side. 0: 512 bytes 1: 500 bytes in GIGA mode
4:0	RO	0	**Reserved**

Offset 7Ah: Chip Configuration Register C (CFG_C)

Configuration for local bus support. To boot BIOS ROM, load from EEPROM at power up. Can be updated by software.

Bit	Attribute	Default	Description
7	RWE	0	**EELOAD.** Enable EEPROM embedded and direct programming, always 0 after power on and loading
6	RWE	0	**BROPT.** Tie the unused boot ROM address MA to Logic 1
5	RWE	0	**DLYEN.** Turn on Delay transaction while memory read boot ROM
4:3	RWE	0	**DL_AKTM[1:0].** Ack DLLP Latency Timer Limit Value 00: 0, send Ack immediately 01: 64 clocks (128 symbols, 0.5us) 10: 128 clocks (256 symbols, 1.0us) 11: 224 clocks (448 symbols, 1.8us)
2:0	RWE	0	**BPS[2:0].** Boot ROM size support selection

BPS[2:0]	(000)	(001)	(010)	(011)	(100)	(101)	110
(K)	0	64	128	256	512	1M	2M

Offset 7Bh: Chip Configuration Register D (CFG_D)

Configuration for PCI capabilities. Load from EEPROM at power up, can be updated by software while MCR1.DIAG = 1.

Bit	Attribute	Default	Description
7	RWE	0	**IODIS.** IO Access Mode Disable.
6:4	RO	0	**Reserved**
3	RWE	0	**HTMRL4.** For interrupt pending control. Reduce time hold-off control when this bit is set to take only low 4 bits to do hold-off mechanism.
2:0	RO	0	**Reserved**

Offset 7Ch: DMA Configuration Register 0 (DCF0)

Configuration for DMA control capabilities. Load from EEPROM at power up, can be updated by software.

Bit	Attribute	Default	Description
7	RWE	0	**SMBSADEN.** Update the SMB slave address while set to 1.
6:3	RWE	0	**SMB_SAD[3:0].** The LSB 4 bits of SMB slave address. The SMB 3 bits are fixed as 001b.
2:0	RO	0	**Reserved**

Offset 7Dh: DMA Configuration Register 1 (DCF1)

Configuration for DMA Control capabilities. Load from EEPROM at power up, can be updated by software.

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RWE	0	**EE_L1DEEP_EN.** L1 Deep Enable.
2:0	RO	0	**Reserved**

Offset 7Eh: MAC Receive Configuration Register 0 (MCFG0)

Configuration for MAC receive control capabilities. Load from EEPROM at power up, can be updated by software.

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RWE	0	**PQEN. ***Enable 802.1p/ 802.1Q tagging function
1	RWE	0	**RTGOPT. ***Option for receiving packet behavior
0	RWE	0	**VIDFR.** Filter out those incoming packet with VLAN_ID mis-matched.

Note:

PQEN	RTGOPT	Behavior
0	0	tx: all packet untagged rx: both untagged/tagged packets(NOT extracting tag)
0	1	tx: all packet untagged rx: ONLY untagged packets.(NOT extracting tag)
1	0	tx: all packet tagged rx: both untagged/tagged packets (Extract tag from tagged packet)
1	1	tx: all packet tagged rx: ONLY tagged packets (Extract tag from tagged packets)

Offset 7Fh: MAC Transmit Configuration Register 1 (MCFG1)

Configuration for MAC transmit control capabilities. Load from EEPROM at power up, can be updated by software.

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RWE	0	**TXQBK[1:0].** Non blocking mode packet threshold control. 00: 64 pkts 01: 32 pkts 10: 128 pkts 11: 8 pkts
1	RWE	0	**TXQNOBK**. Priority transmit Non-blocking mode.
0	RWE	1b	**SNAPOPT**. Control bit for tag insertion on Snap-frame. 1: Tag inserted from 13th byte 0: Tag inserted after SNAP coded.(21th byte)

Offset 81 - 80h: Reserved

Power Management Capability Shadow Register (Offset 82h)

Load from EEPROM at power up, can be updated by software for diagnosis purpose when PMCCDIAG=1.

Offset 82h: Power Management Capability Shadow (PMCC)

Bit	Attribute	Default	Description
7	RE	0	**DSI**.
6	RE	0	**D2_Dis**. Disable D2 power state support.
5	RE	0	**D1_Dis**. Disable D1 power state support.
4	RE	1b	**D3c_En**. D3 cold (D3Aux) power state capable, can inset PME#, while defined wake up event coming.
3	RE	1b	**D3h_En**. D3 hot power state capable, can inset PME#, while defined wake up event coming.
2	RE	1b	**D2_En**. D2 low power state capable, can inset PME#, while D2_Dis = 0, a defined wake up event coming.
1	RE	1b	**D1_En**. D1 low power state capable, can inset PME#, while D1_Dis = 0, a defined wake up event coming.
0	RE	0	**D0_En**. D3 cold (D3Aux) power state capable, can inset PME#, while defined wake up event coming.

Note:
The PMCC capabilities map to PCI PMU extend register are
Dx_EN.Enable PME# report in x power state,
D0_EN = D0_En (PMCC[0].
D1_EN = D1_En & ~D1_Dis. (PMCC[1] & !PMCC[5]).
D2_EN = D2_En & ~D2_Dis. (PMCC[2] & !PMCC[6]).
D3H_EN = D3h_En. (PMCC[3])
D3C_EN = PMCC[4] & VAUXJMP.

PMU Sticky Bit Shadow Register (Offset 83h)

Offset 83h: PMU Sticky Bit Shadow (STKSHDW)

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	0	**STKDS[1:0].** Sticky power state indicator in suspend well. Software must maintain the power state consistency between suspend well and device state.

MIB Counter Control and Status Registers (Offset 84h, 88h – 8Bh)

Offset 84h: MIB Counter Control and Status Register

Initialization
During chip initialization, MIBCR.MIBCLR should be toggled to clear all MIB counters.
Event Accumulation
32 8-bits temporary real-time counters are standby to count up 32 possible network events at the same time.
MIB SRAM Update
When any real-time counter reaches a pre-defined threshold, all those 32 8-bit counters will be flushed into MIB SRAM.
NearFull Warning
When any of MIB SRAM entries reaches a pre-define watermark, an interrupt will be issued (ISR2.MIBFI) to have a near full warning message. The Read-out action is required to avoid those MIB counters overflow

Host Read MIB (Hardware advance SRAM read pointer first and issue embed read)

1. Issue MBTRINI command, HC will reset MIB read pointer and pop index 0 counter value to MIB_DAT port.
2. Software read MIB_DAT port, the MIB_DAT value is previous updated by a embedded read operation and HC will increment the read pointer first and issue new pop for the new pointer and update MIB_DAT.
3. Repeat step-2 till all 32 index is read out (index0 ~ index31).

MIB clear
Software can try to reset all MIB contents by toggling MIBCR.MIBCLR. The event receiver should be blocked and the real-time tmp counter should be also reset.

Bit	Attribute	Default	Description
7	RW0U	0	**MIBISTOK.** MIB BIST Check Status. write clear. 0: Succeed 1: Fail
6	RW	0	**MBISTGO.** Trigger MIB Counter BIST. Work only while DIAG = 1
5	RW	0	**MIBINC.** Increment MIB counter by 1,active only while DIAG = 1; for diagnosis, MIBINC will increase the MIB pointed by current read pointer
4	RW	0	**MIBHI.** MIB Counter Near Full on Higher Condition. 0: 24'h80_0000 1: 24'hc0_0000
3	RW	0	**MIBFREEZE.** Freeze MIB Counter Increment
2	RW	0	**MIBFLUSH.** Force Flush Real Time Counts into MIB SRAM
1	RW	0	**MBTRINI.** Return MIB read pointer to 0, and the MIB embedded logic will read the index-0 MIB counter value to MIB_DAT port. Read as 0 always.
0	RW	0	**MIBCLR.** Clear the MIB SRAM contents. Every time software is up, it needs to issue MIBCLR command to clear internal MIB SRAM.

Note:
Hardware Implementation should freeze the SRAM values when it reaches real Full condition. And avoid continuous NearFull status update when driver is busy.

Offset 8Bh – 88h: MIB Counter Data and Address Output Port Registers (MIBDATA)

VT6130 supports 32-sets 24 bit network event statistics counters for management.

Bit	Attribute	Default	Description
31:24	RO	0	**MIB_Ptr.** MIB Counter Index.
23:0	RO	0	**MIB_Data.** MIB Counter Value

```
if (SMBCMD_PAGE)          REGI88 = SMBCMD;
else if (SMBSTS_PAGE)     REGI88 = SMBSTS;
else                      REGI88 = MIBCOUT
```

MIB Counter Control and Status Registers (Offset 85h)

Offset 85h: EE_SWDATA (EESWDAT)

Bit	Attribute	Default	Description
7:0	RO	0	8-bit EEPROM loaded data. Reserved for software usage.

Offset 87 - 86h: Reserved

Flush ROM Control Registers (Offset 8C – 91h)

Offset 8E ~ 8C: Flush ROM Embedded R/W Address / EEPROM Embedded Write Data Register

Bit	Attribute	Default	Description
23:16	RW	0	**BPMAHHi**
15:8	RW	0	**BPMAHi**
7:0	RW	0	**BPMALo**

Offset 8F: Flush ROM Embedded Write Data Register

Bit	Attribute	Default	Description
7:0	RW	0	**BPMD_w**. Flash ROM Embedded write data port. Read data port is located at offset 91h.

Note: 8-bit Flash ROM is supported.

Offset 90h: Flash ROM Embedded Control and Status Register (BPCMD)

Bit	Attribute	Default	Description
7	RU	1b	**BPDNE.** Reset as 1, clear while EBPWR is set and set as 1 while command issued to boot ROM
6:4	RO	0	**Reserved**
3	RW	0	**EBPWEN.** SPI Flush embedded Write Enable command.
2	RW	0	**EBPWDI.** SPI Flush embedded Write Disable command.
1	RW	0	**EBPWR.** Boot ROM embedded write command
0	RW	0	**EBPRD.** Boot ROM embedded read command

Note: BPRD/BPWR cannot issue at the same time. Must be in sequence

Offset 91h: Flush ROM Embedded Read Data Port Register (BPMD_r)

Bit	Attribute	Default	Description
7:0	RW	0	**BPMD_r.** Flash ROM Embedded Read data port. Write data port is located at offset 8Eh

Note: 8-bit Flash ROM is supported.

EEPROM Control Registers (Offset 92h – 97h)

Offset 92h: EPROM Checksum Field Shadow Register (EEChkSum)

CheckSum shadow of EEPROM contents. Load from EEPROM at power up for software reference.

Bit	Attribute	Default	Description
7:0	RE	0	**EEChkSum.** EEPROM checksum fielder shadow.

Offset 93h: EEPROM Embedded Control and Status Register (EECSR)

VT6130 supports 4-wire serial EEPROM like 93c06, 93c46. The embedded controller provides the capability.

- **Dynamic Reload** to restore the related configurations and Ethernet ID
- **Embedded read or write** EEPROM in word basis
- **Direct Programming** read write EEPROM for manufacturing purpose

Bit	Attribute	Default	Description
7	RW	0	**SPIDPM.** Enable SPI Flush Direct Program Mode.
6	RW	0	**EMBP.** EEPROM Embedded Program mode enable. Programmable only when CFGC.EELOAD=1.
5	RWC	0	**RELOAD.** Dynamic reload EEPROM. The Ethernet ID and related chip configuration will be updated
4	RW	0	**DPM.** EEPROM Direct Program mode enable. Programmable only when CFGB.EELOAD=1
3	RW	0	**ECS.** DPM EEPROM interface CS output
2	RW	0	**ECK.** DPM EEPROM interface CK output
1	RW	0	**EDI.** DPM EEPROM interface DI output
0	RO	0	**EDO.** DPM EEPROM interface DO status

Offset 95h – 94h: EEPROM Embedded Read Data Port Register (EE_RD_DATA)

Bit	Attribute	Default	Description
15:0	RW	0	**EE_RD_DATA.** EEPROM Embedded Read data port. Write data port is located at offset 8C - 8Dh

Offset 96h: EEPROM Embedded Read Address Port Register (EADDR)

93c06/93c46/93c56 are supported.

Bit	Attribute	Default	Description
7:0	RW	0	**EEADDR[7:0]**. EEPROM Embedded Operation Address Port.

Offset 97h: EEPROM Embedded Control and Status Register (EMCMD)

Bit	Attribute	Default	Description
7	RU	1b	**EDONE.** Embedded read/write done 0: EMBEEWDI|EMBEEWEN|EMBEERD are set 1: Embedded program done
6:4	RO	0	**Reserved**
3	RWC	0	**EWDIS.** Embedded program EEPROM into write disable mode; cleared by the macro while program done
2	RWC	0	**EWEN.** Embedded program EEPROM into write enable mode; cleared by the macro while program done
1	RWC	0	**EWR.** Embedded write with programmable address, cleared by the macro while program done
0	RWC	0	**ERD.** Embedded read with programmable address, cleared by the macro while program done

Note:
EEPROM write operation must follow the sequence:
EEWEN → EEWR → EEWR ……. → EEWDIS

Configuration Status Registers (Offset 98h – 9Bh)

Offset 98h: Jumper Strapping Status Register 0 (JMPSR0)

Programmable only while MCR1.DIAG = 1

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved.**
0	RO	0	**TESTM0.** Mode Control Pin Status.

Offset 99h: Chip Configuration Status Register 1 (JMPSR1)

Bit	Attribute	Default	Description
7:3	RO	0	**GSUSPRZ**
6	RO	0	**Reserved**
5	RO	0	**J_EEDIS**
4:3	RO	0	**Reserved**
2	RO	0	**J_VEESEL.** Strapping Status of Virtual EEPROM
1	RO	0	**Reserved**
0	RO	0	**J_SPI.** Strapping Status of SPI and Legacy BROM.

Offset 9Ah: Chip Configuration Status Register 2 (JMPSR2)

Bit	Attribute	Default	Description
7	RO	0	**GMCFG1**
6	RO	0	**GMCFG0**
5	RO	0	**GTCFG2**
4	RO	0	**GTCFG1**
3	RO	0	**GTCFG0**
2:0	RO	0	**Reserved**

Offset 9Bh: Media Jumper Strapping Status Register 3 (MJMPSR)

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**MODE1000**
3	RO	0	**MODE100**
2	RO	0	**MASTER**
1	RO	0	**ANEGDIS**
0	RO	0	**FRCDPLX**

Chip Operation and Diagnosis Status Register (Offset 9Ch)

Offset 9Ch: Chip Operation and Diagnosis Status Register (CHIPGSR)

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RO	0	**RTBISTOK.** Power on Reset Generator Self Test Status
4	RO	0	**EEPR.** EEPROM load complete indication during power up sequence and 73h is detected.
3:1	RO	0	**Reserved**
0	RO	0	**PMU10.** PMC Support Version. EEPROM loaded status

Offset 9E - 9Dh – Reserved

Chip Operation and Diagnosis Control Register (Offset 9Fh)

Offset 9Fh: Chip Operation and Diagnosis Control Register (CHIPGCR)

Bit	Attribute	Default	Description
7	RW	0	**FCGMII.** While FCMODE =1, Software force MAC operating on GMII mode, else operating in MII mode.
6	RW	0	**FCFDX.** Software force MAC operating on Full Duplex mode. Available only while FCMODE = 1.
5	RO	0	**Reserved**
4	RW	0	**FCMODE**. Program MAC side into force mode
3	RO	0	**Reserved**
2	RW	0	**TM1US.** Software Timer 1 in micro-second resolution.
1	RW	0	**TM0US.** Software Timer 0 in micro-second resolution.
0	RO	0	**Reserved**

Note:
Offset 9F[7:6, 4] (FCGMII, FCFDX, FCMODE) must be located in suspend well.
In FCMODE, the MAC will operate in the setting mode; ignore the PHY priority resolution result get by auto-polling.

Wake On Lan Registers (Offset A0h – ADh)

Offset A0h: Wake On Lan Event Enable Set Register (WOLCR0.s)

Offset A4h: Wake On Lan Event Enable Control Register (WOLCR0.c)

For set port, write 1 means Set to 1; write 0 has no effect.
For clear port, write 1 means Clear to 0; write 0 has no effect; read value is as same as Set port.

Bit	Attribute	Default	Description
7	RW1	0	**PTNMH7.** Enable WOL event detection of Patten Match, pattern #7
6	RW1	0	**PTNMH6.** Enable WOL event detection of Patten Match, pattern #6.
5	RW1	0	**PTNMH5.** Enable WOL event detection of Patten Match, pattern #5
4	RW1	0	**PTNMH4.** Enable WOL event detection of Patten Match, pattern #4
3	RW1	0	**PTNMH3.** Enable WOL event detection of Patten Match, pattern #3
2	RW1	0	**PTNMH2.** Enable WOL event detection of Patten Match, pattern #2
1	RW1	0	**PTNMH1.** Enable WOL event detection of Patten Match, pattern #1
0	RW1	0	**PTNMH0.** Enable WOL event detection of Patten Match, pattern #0

Offset A1h: Wake On Lan Event Enable Set Register (WOLCR1.s)

Offset A5h: Wake On Lan Event Enable Control Register. (WOLCR1.c)

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW1	0	**LinkOffEn.** Enable WOL event detection for, link On to Link Fail.
2	RW1	0	**LinkOnEn.** Enable WOL event detection for, link Fail to Link On.
1	RW1	0	**MagicEn.** Enable WOL event detection for Magic Packet.
0	RW1	0	**UniQEN.** Enable WOL event detection for receiving an unicast packet with recognized Ethernet address.

Offset A2h: Power Management Configuration Set Register (PWCFG.s)

Offset A6h: Power Management Configuration Control Register (PWCFG.c)

Internal updated by hardware control for Wake-On-Lan events are detected.
Write 1 means set for testing purpose. Write 0 has no effect

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW1S	0	**PME_SR**. PMCSR PME_SR shadow. For testing purpose
2	RW1S	0	**PME_EN.** PMCSR, PME_EN shadow.
1:0	RO	0	**Reserved**

Offset A3h: Wake-On-Lan Configuration Set Register (WOLCFG.s)

Offset A7h: Wake-On-Lan Configuration Control Register (WOLCFG.c)

1. All filtering results will be qualified with RXOKEOF, in WOL mode PROM=0, SEP=0, AR=0, RXOKEOF = normal_accept in AB=1,AM=1 & accept Physical packet
2. Whenever power statuses are set, the Receiver will be blocked until software interleaving to turn on the receiver again.
3. When entering WOL detected state receiver, packet accepting is controlled by SAB /SAM/RXOKEOF.

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW1S	0	**LED_OFF.** Used to turn off all LEDs. While enabled, all LEDs will be dark.
5	RW1	0	**SAM.** Accept multicast packet in power mode.
4	RW1S	0	**SAB.** Accept Broadcast packet in power mode.
3:0	RO	0	**Reserved**

Offset A8h: Wake On Lan Event Status Set Register (WOLSR0.s)

Offset ACh: Wake On Lan Event Status Control Register (WOLSR0.c)

Internal updated by hardware control for Wake On Lan events are detected
Write 1 means set for testing purpose. Write 0 has no effect.

Bit	Attribute	Default	Description
7	RW1S	0	**PTNMH7Int.** WOL event detected of Patten Match, pattern #7
6	RW1S	0	**PTNMH6Int.** WOL event detected of Patten Match, pattern #6
5	RW1S	0	**PTNMH5Int.** WOL event detected of Patten Match, pattern #5
4	RW1S	0	**PTNMH4Int.** WOL event detected of Patten Match, pattern #4
3	RW1S	0	**PTNMH3Int.** WOL event detected of Patten Match, pattern #3
2	RW1S	0	**PTNMH2Int.** WOL event detected of Patten Match, pattern #2
1	RW1S	0	**PTNMH1Int.** WOL event detected of Patten Match, pattern #1
0	RW1S	0	**PTNMH0Int.** WOL event detected of Patten Match, pattern #0

Offset A9h: Wake On Lan Event Status Set Register. (0xA9h, WOLSR1.s)

Offset ADh: Wake On Lan Event Status Control Register. (0xADh, WOLSR1.c)

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW1S	0	**LinkOffInt.** WOL event detected form link On to Link Off.
2	RW1S	0	**LinkOnntI.** WOL event detected form link Off to Link On.
1	RW1S	0	**MagicInt.** WOL event detected for Magic Packet.
0	RW1S	0	**UniQEnInt.** WOL event detected for receiving an unicast packet with recognized Ethernet address.

Groups of 16-bits CRC Register (Offset B0h - BFh)

Those CRC value are all pre-defined for pattern match packet Wakeup usage.

Offset B3h ~ B0h

Bit	Attribute	Default	Description
31:16	RW	0	**Pattern Match group 1 CRC16 value**
15:0	RW	0	**Pattern Match group 0 CRC16 value**

Offset B7h ~ B4h

Bit	Attribute	Default	Description
31:16	RW	0	**Pattern Match group 3 CRC16 value**
15:0	RW	0	**Pattern Match group 2 CRC16 value**

Offset BBh ~ B8h

Bit	Attribute	Default	Description
31:16	RW	0	**Pattern Match group 5 CRC16 value**
15:0	RW	0	**Pattern Match group 4 CRC16 value**

Offset BFh ~ BCh

Bit	Attribute	Default	Description
31:16	RW	0	**Pattern Match group 7 CRC16 value**
15:0	RW	0	**Pattern Match group 6 CRC16 value**

8 Groups of 128 bit Pattern Match Bit Mask Register (Offset C0h – FFh)

Those bit masks value are all pre-defined for pattern match packet Wakeup usage.
2 pages selected by {CAMCR.PS0, CAMCR.PS1}

Offset CF – C0h

Bit	Attribute	Default	Description
127:96	RW	0	**Pattern Match group 0/4 bit mask [127:96]**
95:64	RW	0	**Pattern Match group 0/4 bit mask [95:64]**
63:32	RW	0	**Pattern Match group 0/4 bit mask [63:32]**
31:0	RW	0	**Pattern Match group 0/4 bit mask [31:0]**

Offset DF – D0h

Bit	Attribute	Default	Description
127:96	RW	0	**Pattern Match group 1/5 bit mask [127:96]**
95:64	RW	0	**Pattern Match group 1/5 bit mask [95:64]**
63:32	RW	0	**Pattern Match group 1/5 bit mask [63:32]**
31:0	RW	0	**Pattern Match group 1/5 bit mask [31:0]**

Offset EF – E0h

Bit	Attribute	Default	Description
127:96	RW	0	**Pattern Match group 2/6 bit mask [127:96]**
95:64	RW	0	**Pattern Match group 2/6 bit mask [95:64]**
63:32	RW	0	**Pattern Match group 2/6 bit mask [63:32]**
31:0	RW	0	**Pattern Match group 2/6 bit mask [31:0]**

Offset FF – F0h

Bit	Attribute	Default	Description
127:96	RW	0	**Pattern Match group 3/7 bit mask [127:96]**
95:64	RW	0	**Pattern Match group 3/7 bit mask [95:64]**
63:32	RW	0	**Pattern Match group 3/7 bit mask [63:32]**
31:0	RW	0	**Pattern Match group 3/7 bit mask [31:0]**

MII Registers

Offset 00h: Mode Control

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RW SC	0	0 (SC)	**Software Reset.** 0: Normal operation 1: PHY software reset
14	RW	0	0	**Loopback** 0: Disable loop back mode 1: Enable loop back mode
13	RW	0	N/A	**Speed Selection (LSB)** Please refer to bit 6 for detailed information
12	RW	1b	N/A	**Auto-Negotiation Enable** 0: Disable Auto-Negotiation Process 1: Enable Auto-Negotiation Process
11	RW	0	0	**Power Down** 0: Normal operation 1: Power down
10	RW	0	0	**Isolation** 0: normal operation 1: Isolate PHY from MII, GMII, or RGMII electrically
9	RW SC	0	SC	**Restart Auto-Negotiation** 0: Normal operation 1: Restart Auto-Negotiation Process
8	RW	1b	N/A	**Duplex Mode** 0: Half duplex 1: Full duplex
7	RW	0	0	**Collision Test Enable** 0: Disable COL signal test 1: Enable COL signal test
6	RW	1b	0	**Forced Speed Selection.** Bit 6 Bit 13 0 0 10Mbps 0 1 100Mbps 1 0 1000Mbps 1 1 Reserved
5:0	RO	0	0	**Reserved**

Offset 01h: Status

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RO	0	0	**100BASE-T4 Capability** 0: PHY not able to perform 100BASE-T4 1: PHY able to perform 100BASE-T4
14	RO	1b	1b	**100BASE-X Full Duplex Capability** 0: PHY not able to perform full duplex 100BASE-X 1: PHY able to perform full duplex 100BASE-X
13	RO	1b	1b	**100BASE-X Half Duplex Capability** 0: PHY not able to perform half duplex 100BASE-X 1: PHY able to perform half duplex 100BASE-X
12	RO	1b	1b	**10BASE-T Full Duplex Capability** 0: PHY not able to operate at 10Mb/s in full duplex mode 1: PHY able to operate at 10Mb/s in full duplex mode
11	RO	1b	1b	**10BASE-T Half Duplex Capability** 0: PHY not able to operate at 10 Mb/s in half duplex mode 1: PHY able to operate at 10 Mb/s in half duplex mode
10	RO	0	0	**100BASE-T2 Full Duplex Capability** 1: PHY able to perform full duplex 100BASE-T2 0: PHY not able to perform full duplex 100BASE-T2
9	RO	0	0	**100BASE-T2 Half Duplex Capability** 1: PHY able to perform half duplex 100BASE-T2 0: PHY not able to perform half duplex 100BASE-T2
8	RO	1b	1b	**Extended Status** 0: No extended status information in Register 15 1: There is extended status information in Register 15
7	RO	0	0	**Reserved**
6	RO	1b	1b	**Preamble Suppression Capability** 0: PHY does not accept management frames with preamble suppressed 1: PHY accepts management frames with preamble suppressed.
5	RO	0	0	**Auto-Negotiation Complete** 0: Auto-Negotiation process not completed 1: Auto-Negotiation process completed
4	RO LH	0	0	**Remote Fault.** 0: No remote fault condition detected 1: Remote fault condition detected
3	RO	1b	1b	**Auto-Negotiation Capability** 0: PHY is not able to perform Auto-Negotiation 1: PHY is able to perform Auto-Negotiation
2	RO LL	0	0	**Link Status** 0: Link is down 1: Link is up
1	RO LH	0	0	**Jabber Detect** 0: No jabber condition detected 1: Jabber condition detected
0	RO	1b	1b	**Extended Capability** 0: Support basic register set capabilities only 1: Support extended register capabilities

Offset 02h: PHY Identifier Register #1

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15:0	RO	0243		**Organizationally Unique Identifier [18:3]**

Offset 03h: PHY Identifier Register #2

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15:10	RO	000011b		**Organizationally Unique Identifier [24:19]**
9:4	RO	011001b		**Vendor Model Number**
3:0	RO	0000b		**Vendor Revision Number**

Offset 04h: Auto-Negotiation Advertisement

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RW	1b	0	**Next-Page Transmission Request** 0: Next pages are not supported 1: Next pages are supported
14	RO	0	0	**Reserved**
13	RW	0	0	**Transmit Remote Fault** 0: Not advertise remote fault detection capability 1: Advertise remote fault detection capability
12	RW	0	0	**Reserved technologies**
11	RW	0	0	**Advertise Asymmetric Pause** 0: Asymmetric flow control is not supported 1: Asymmetric flow control is supported
10	RW	0	0	**Pause** 0: Flow control is not supported 1: Flow control is supported
9	RO	0	0	**Advertise 100BASE-T4 Capability** 0: 100Base-T4 not supported 1: 100Base-T4 is supported
8	RW	1b	1b	**Advertise 100BASE-TX Full Duplex** 0: 100Base-TX full duplex not supported 1: 100Base-TX full duplex is supported
7	RW	1b	1b	**Advertise 100BASE-TX Half Duplex** 0: 100Base-TX half duplex not supported 1: 100Base-TX half duplex is supported
6	RW	1b	1b	**Advertise 10BASE-T Full Duplex** 0: 10Base-T half duplex not supported 1: 10Base-T half duplex is supported
5	RW	1b	1b	**Advertise 10BASE-T Half Duplex** 0: 10Base-T full duplex not supported 1: 10Base-T full duplex is supported
4:0	RO	00001b	00001b	**Advertise Selector Field**

Offset 05h: Auto-Negotiation Link Partner Ability

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RO	0	0	**Next Page** 0: Next pages are not supported by link partner. It is Received Code Word Bit 15. 1: Next pages are supported by link partner
14	RO	0	0	**Acknowledge** 0: no acknowledgement 1: link partner acknowledges reception of local node's capability It is Received Code Word Bit 14.
13	RO	0	0	**Remote Fault** 0: link partner does not indicate a remote fault 1: link partner is indicating a remote fault It is Received Code Word Bit 13.
12	RO	0	0	**Reserved**
11	RO	0	0	**Advertise Asymmetric Pause** 0: asymmetric flow control is NOT supported by Link partner 1: asymmetric flow control is supported by Link partner
10	RO	0	0	**PAUSE** 0: flow control is not supported by Link partner 1: flow control is supported by Link partner
9	RO	0	0	**100BASE-T4** 0: 100Base-T4 not supported by link partner 1: 100Base-T4 is supported by link partner
8	RO	0	0	**100BASE-TX Full Duplex** 0: 100Base-TX full duplex not supported by link partner 1: 100Base-TX full duplex is supported by link partner
7	RO	0	0	**100BASE-TX Half Duplex** 0: 100Base-TX not supported by link partner 1: 100Base-TX is supported by link partner
6	RO	0	0	**10BASE-T Full Duplex** 0: 10Base-T full duplex not supported by link partner 1: 10Base-T full duplex is supported by link partner
5	RO	0	0	**10BASE-T Half Duplex** 0: 10Base-T not supported by link partner 1: 10Base-T is supported by link partner
4:0	RO	0	0	**Selector Field**

Offset 06h: Auto-Negotiation Expansion

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15:5	RO	0	0	**Reserved**
4	RO	0	0	**Parallel Detection Fault** 0: A fault has not been detected via Parallel Detection function 1: A fault has been detected via Parallel Detection function
3	RO	0	0	**Link Partner Next-Page Able** 0: Link Partner does not support Next Page 1: Link Partner supports Next Page
2	RO	1b	0	**Local PHY Next-Page Able** 0: Local device does not support Next Page 1: Local device supports Next Page
1	RO LH	0	0	**Page Received** 0: A new page has not been received 1: A new page has been received
0	RO	0	0	**Link Partner Auto-Negotiation Able** 0: Link partner does not support Auto-Negotiation 1: Link partner supports Auto-Negotiation

Offset 07h: Auto-Negotiation Next-Page Transmit Register

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RW	0	0	**Next Page.** Transmit Code Word Bit 15
14	RO	0	0	**Reserved.** Transmit Code Word Bit 14
13	RW	1b	1b	**Message Page.** Transmit Code Word Bit 13
12	RW	0	0	**Acknowledge 2.** Transmit Code Word Bit 12
11	RO	0	0	**Toggle.** Transmit Code Word Bit 11
10:0	RW	001h	001h	**Message/Unformatted Code.** Transmit Code Word Bit 10:0

Offset 08h: Auto-Negotiation Link Partner Next Page Register

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RO	0	0	**Next Page.** Receive Code Word Bit 15
14	RO	0	0	**Acknowledge.** Receive Code Word Bit 14
13	RO	0	0	**Message Page.** Receive Code Word Bit 13
12	RO	0	0	**Acknowledge 2.** Receive Code Word Bit 12
11	RO	0	0	**Toggle.** Receive Code Word Bit 11
10:0	RO	0	0	**Message/Unformatted Code.** Receive Code Word Bit 10:0

Offset 09h: 1000BASE-T Control Register

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15:13	RW	000b	000b	**Transmitter Test Mode.** This test is valid only in 1000BASE-T mode. Refer to IEEE 802.3-2002, section 40.6.1.1.2 for more information. 000: Normal Mode 001: Test Mode 1 – Transmit waveform test 010: Test Mode 2 – Transmit jitter test in MASTER mode 011: Test Mode 3 – Transmit jitter test in SLAVE mode 100: Test Mode 4 – Transmit distortion test Others: Reserved
12	RW	0	0	**MASTER/SLAVE Manual Configuration Enable** 0: Disable MASTER/SLAVE Manual Configuration value 1: Enable MASTER/SLAVE Manual Configuration value
11	RW	0	0	**MASTER/SLAVE Manual Configuration Value** 0: Configure PHY as SLAVE during MASTER/SLAVE negotiation 1: Configure PHY as MASTER during MASTER/SLAVE negotiation This bit is only valid when bit 12 is set to 1.
10	RW	1b	0	**Port Type** 0: Single-port device (SLAVE) 1: Multi-port device (MASTER)
9	RW	1b	0	**1000BASE-T Full Duplex Capability** 0: Not advertise 1: Advertise 1000BASE-T full duplex capable
8	RW	1b	0	**1000BASE-T Half Duplex Capability** 0: Not advertise 1: Advertise 1000BASE-T half duplex capable
7:0	RO	0	0	**Reserved**

Offset 0Ah: 1000BASE-T Control Register

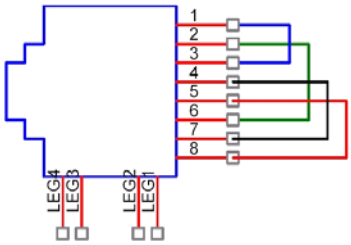
Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RO LH SC	0	0	**MASTER/SLAVE Configuration Fault** 0: No MASTER/SLAVE configuration fault detected 1: MASTER/SLAVE configuration fault detected
14	RO	0	0	**MASTER/SLAVE Configuration Resolution** 0: Local PHY configuration resolved to SLAVE 1: Local PHY configuration resolved to MASTER
13	RO	0	0	**Local Receiver Status** 0: Local receiver not OK 1: Local receiver OK
12	RO	0	0	**Remote Receiver Status** 0: Remote receiver not OK 1: Remote receiver OK
11	RO	0	0	**Link Partner 1000BASE-T Full Duplex Capability** 0: Link Partner not 1000BASE-T full duplex capable 1: Link Partner 1000BASE-T full duplex capable
10	RO	0	0	**Link Partner 1000BASE-T Half Duplex Capability** 0: Link Partner not 1000BASE-T half duplex capable 1: Link Partner 1000BASE-T half duplex capable
9:8	RO	0	0	**Reserved**
7:0	RO	0	0	**Idle Error Count**

Offset 0B – 0Eh: Reserved

Offset 0Fh: Extended Status

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RO	0	0	**1000BASE-X Full Duplex Capability** 0: PHY is not 1000BASE-X full duplex capable 1: PHY is 1000BASE-X full duplex capable
14	RO	0	0	**1000BASE-X Half Duplex Capability** 0: PHY is not 1000BASE-X half duplex capable 1: PHY is 1000BASE-X half duplex capable
13	RO	1b	1b	**1000BASE-T Full Duplex Capability** 0: PHY is not 1000BASE-T full duplex capable 1: PHY is 1000BASE-T full duplex capable
12	RO	1b	1b	**1000BASE-T Half Duplex Capability** 0: PHY is not 1000BASE-T half duplex capable 1: PHY is 1000BASE-T half duplex capable
11:0	RO	0	0	**Reserved**

Offset 10h: PHY Specific Control Register #1

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RW	0	NA	**MstExtLpBk.** This function is designed for manufacturing and debugging. The connect type of external loopback connector is constructed as the following figure. This function can be enabled by setting logic 1 to this bit. 
14	RW	1b	NA	**NwyFrc2FullEn.** When the link partner is working on force mode and VT6130 is working on NWAY mode, VT6130 will have priority to operate on full-duplex. If this bit is set to logic 0, then VT6130 will operate on half-duplex.
13	RW	0	NA	**ForceLink.** This function is designed for waveform testing. When the function enabled by setting logic 1 to this bit, GPHY will output TX waveform no matter what the link status is.
12	RO	1b	NA	**Reserved** (Do not program)
11	RW	1b	NA	**Smart Speed.** 0: No Downshift 1: Downshift to 100Mbps when 1000Mbps link fails.
10	RW	0	NA	**Heart Beat.** 0: Disable 1: Enable
9	RW	1b	NA	**Jabber** 0: Disable 1: Enable
8	RW	0b	NA	**CK125ManualConfiguration** The output clock for IEEE 802.3 clause 40.6 jitter measure can manual configure. 1: Manual Configuration Enabled. 0: Manual Configuration Disabled.
7	RW	1	NA	**CK125IsMaster** When the output clock for IEEE 802.3 clause 40.6 jitter measure manual configure enable. 1: Manual Configure for Master clock output. 0: Manual Configure for Slave clock output.
6:5	RO	01b	NA	**Reserved** (Do not program)
4:3	RO	01b	NA	**Reserved** (Do not program)
2	RW	0	NA	**Repeater Mode.** 0: Disable 1: Enable
1:0	RO	0	NA	**Reserved**

Offset 11h: PHY Link Status

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15	RO	0	0	**Link Status** 0: Link down 1: Link up
14:13	RO	00b	00b	**Link Speed** 00: Link at 10Base-T 01: Link at 100Base-TX 10: Link at 1000Base-T 11: Reserved It is only valid when bit 15 is 1.
12	RO	0	0	**Link Duplex** 0: link at half duplex 1: link at full duplex It is only valid when bit 15 is 1.
11	RO	0	0	**MDI/MDIX** 0: MDI 1: MDIX
10	RO	0	0	**APS Sleep** 0: Normal operation 1: APS sleep mode is entered
9	RO	0	0	**Jabber Detected** 0: 10Base Jabber not detected 1: 10Base Jabber detected
8:0	RO	0	0	**Reserved**

Offset 12 – 13h: Reserved

Offset 14h: PHY Specific Control Register #2

Bit	Attribute	Default		Description
		HW Reset	SW Reset	
15:12	RO	0	NA	**Reserved**
11	RW	1b	NA	**APS_ON**. Used to activate auto power saving (APS) mode 0: Disable APS 1: Enable APS
10	RO	1b	NA	**Reserved** (Do not program)
9	RW	0	NA	**MDIX.** When disable auto-crossover 0: MDI 1: MDIX
8:7	RW	10b	NA	**FIFO_Depth.** FIFO depth latency 00: latency = 2 01: latency = 3 10: latency = 4 11: latency = 5
6	RW	1b	NA	**Speed 10 to 100 Enable**. Detect the link partner speed change from 10BASE-T to 100BASE-TX by detecting MLT3 signals. 1: Enable 0: Disable
5:3	RO	101b	NA	**Reserved.** Do not program.
2	RW	1b	NA	**Auto-crossover Enable** 0: Disable auto MDI/MDIX 1: Enable auto MDI/MDIX
1	RW	1b	NA	**EnDSPRegChg.** When this bit is enabled, then some DSP registers will be asserted to different parameters for different link status.
0	RO	1b	NA	**Reserved** (Do not program)

Offset 1F – 15h: Reserved

User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

FUNCTIONAL DESCRIPTIONS

Buffer Management

The VT6130 hardware controller and drivers communicate through two data structures:

- Control and status register (CSR)
- Descriptor entries and data buffers

During initialization, drivers create the structure of the transmit and receive descriptors in physical memory and decide base address for the receive and transmit descriptor rings. They are written to CSR18 (Desc_Base_Add_Hi) for common Tx/Rx higher 32 bits address and CSR38 (RD_Base_Lo) for Rx lower 32 bits address, CSR40 (TD0_Base_Lo), CSR (TD1_Base_Lo), CSR48 (TD2_Base_Lo), CSR4C (TD3_Base_Lo) for TD queue 0 ~ 3 respectively. The number of entries contained in the descriptor rings and the buffer reserved in the physical memory for TD/RD are set up.

Each descriptor entry must occupy a contiguous area of memory. The Receive (Transmit) Descriptor DMA register of CSR also keeps the content of current and next receive (Transmit) Descriptor.

For reception, the controller receives data frames in Rx FIFO and updates the status information of receive Descriptor DMA Register after reception is complete. It then proceeds to write back to descriptor in memory and bring data back using one DMA cycle.

For transmission, the controller starts the DMA cycle and brings the data from memory to Tx FIFO. Lately update the status information of Transmission Descriptor DMA register after transmission complete and then proceed to write back to descriptor in memory using another DMA cycle.

Descriptor Information

Transmit Descriptor Command Block Format

Each command block define a transmit packet with buffer segmentation

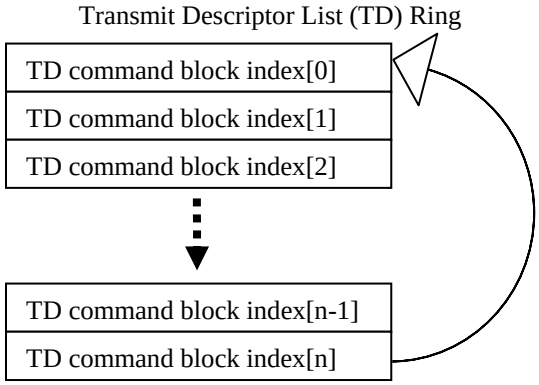


Table 7. Tx Descriptor Command Block Structure

TD+00	O		TX_Packet_Size[13:0]										TSR1		TSR0	
TD+04	CMDZ			TCR1		TCR0							PQINF[15:0]			
TD+08	Tx_Data_Buffer_Address0.Lo															
TD+0c	Q			Tx_Buffer_Size0[13:0]									Tx_Data_Buffer_Address0.Hi			
TD+10	Tx_Data_Buffer_Address1.Lo															
TD+14	Tx_Buffer_Size1[13:0]												Tx_Data_Buffer_Address1.Hi			
TD+18	Tx_Data_Buffer_Address2.Lo															
TD+1c	Tx_Buffer_Size2[13:0]												Tx_Data_Buffer_Address2.Hi			
TD+20	Tx_Data_Buffer_Address3.Lo															
TD+24	Tx_Buffer_Size3[13:0]												Tx_Data_Buffer_Address3.Hi			
TD+28	Tx_Data_Buffer_Address4.Lo															
TD+2c	Tx_Buffer_Size4[13:0]												Tx_Data_Buffer_Address4.Hi			
TD+30	Tx_Data_Buffer_Address5.Lo															
TD+34	Tx_Buffer_Size5[13:0]												Tx_Data_Buffer_Address5.Hi			
TD+38	Tx_Data_Buffer_Address6.Lo															
TD+3c	Tx_Buffer_Size6[13:0]												Tx_Data_Buffer_Address6.Hi			

Note.

1. Access principle: fetch 8DW each time, and more condition to fetch another 8 DW.
2. TD must be allocated in 16-quadlets base address.
3. We maintain the Hi data buffer address in separate register from [63:48].
4 Each command block define a packet within 7 data segments.

TD Command Block Header 0 Field (Offset 03-00h)

Bit	Description	Updated by
31	**OWN.** Software maintained TD owner ship information, WBTSR will be written back while support signal write back per packet option.	DRV/HC
30	**QUE. List Queuing Indicator** 0: List end 1: Not List end	DRV/HC
29:16	**TxPktSize[13:0].** TCP large send per segment packet size control fields. When write back, these fields are reserved for more status.	DRV/HC
15	**TERR.** Tx Error Status. TERR=ABT|GOWC|OWT|SHDN	HC
14	**FDX.** Current Transaction is serviced by Full Duplex mode	HC
13	**GMII.** Current Transaction is served by GMII mode else MII mode	HC
12	**LNKFL. "1" means packet serviced during link down.**	HC
11	**Reserved.**	HC
10	**SHDN.** "1" means shut down case, no guarantee for Tx ok.	HC
9	**CRS.** Carrier Sense lost detection.	HC
8	**CDH.** Collision Heart beat detection failure in half duplex.	HC
7	**ABT.** Transmission Abort because of excessive Collision	HC
6	**OWT.** Jumbo Frame Tx Abort.	HC
5	**OWC.** Out of window Collision.	HC
4	**COLS.** Collision seen in current good transmission o.k status.	HC
3:0	**NCR[3:0].** Collision Counts in current good transmission o.k status	HC

Note:
1. Jumbo frame in 10/100 mode.
2. In normal case, The TxPktSize is filled by software as "'h0". But in TCP large send case this field is an information update from SC of maximum size of every packet segment.

TD Command Block Header 0 Field (Offset 07-04h)

Bit	Description	Updated by
31:28	**CMDZ[3:0].** CMDZ is to determine how many segments inside the command block (segment number =CMDZ-1)	DRV
27:26	**Reserved.**	DRV
25:24	**TCPLS_SOF, TCPLS_EOF.** 11: Normal Packet. 10: Start of TCP Large Send Descriptor 00: Intermediate TD of a Large Packet 01: End of TCP Large Send Descriptor.	DRV
23	**TIC.** Request to issue interrupt while this packet status is transferred to TD wrk information ring	DRV
22	**PIC.** Priority Interrupt Request. Make sure INTA# is issued over adaptive interrupt scheme	DRV
21	**VETAG.** Enable VLAN TAG. Combine with HC control to insert VLAN tag.	DRV
20	**IPCK.** Request IP checksum calculation.	DRV
19	**UDPCK.** Request UDPP checksum calculation.	DRV
18	**TCPCK.** Request TCP checksum calculation.	DRV
17	**JMBO.** Indicated that a jumbo packet, to disconnect with burst frame, in Gmac side	DRV
16	**CRC.** Disable CRC generation in this packet	DRV
15:13	**Pri[2:0].** 802.1p priority bits	DRV
12	**CFI.** Reserved control bit	DRV
11:0	**VLAN_ID[11:0].** 802.1q Virtual Lan Identifier	DRV

Receive Descriptor Command Block Format

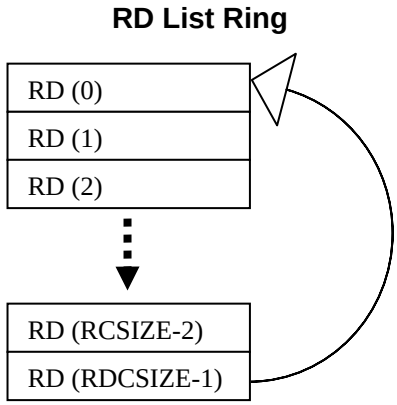


Table 8. Receive Descriptor Format (RD)

RDE0	**O**		**RMBC[13:0]**	**RSR1**	**RSR0**
RDE1	**IPKT**		**CSM**	**PQTAG**	
RDE2	**RX_DATA_BUFFER_ADDRESS.Lo**				
RDE3	**I**	**RX_Buffer_Size[13:0]**		**RX_ DATA_BUFFER_ADDRESS.Hi**	

RD Command Block Header 0 Field (Offset 03 - 00h)

Bit	Description	Updated by
31	**OWN.** Software maintained RD owner ship information, OWN=1 DESC owned by NIC, "0" owned by host	DRV/HC
30	**SHDN.** Shut down case	HC
29:16	**RMBC[13:0].**	HC
15	**RXOK.** Rx receives o.k status.	HC
14	**PFT.** Perfect filtering address match, check the PQTAG encode to see if interesting packet hit	HC
13	**MAR.** NIC accept multicast address packet	HC
12	**BAR.** NIC accept broadcast address packet	HC
11	**PHY.** NIC accept unicast address packet	HC
10	**VTAG.** 802.1p/1q tagging packet indicator	HC
9:8	**STP,EDP. STP. Packet Start, in Desc ring structure** 00: Single packet in Single RD 10: Start of Chained Packet 11: Intermediate segments of chained packet 01: End of Chained Packet	HC
7	**DETAG.** HC de-tag indicator.	HC
6	**SNTAG.**	HC
5	**RXER.** PCS Symbol Error	HC
4	**RL.** Receive Length Error Indication.	HC
3	**CE.** Receive Check Sum Error Indication.	HC
2	**FAE.** Receive Frame Alignment Error Indication.	HC
1	**CRC.** Receive CRC Error Indication.	HC
0	**VIDM.** VID Filtering Miss	HC

RD Command Block Header 1 Field (Offset 07 - 04h)

Bit	Description	Updated by
31:30	**Reserved.**	HC
29:24	**IPTn.** Indexed 64 bit perfect and interesting packet filtering Normally we use CAM 32 ~ 63 as interesting packet filtering	HC
23	**Reserved.**	HC
22	**IPOK.** NIC IP checksum validation ok.	HC
21	**TUPOK.** NIC TCP/UDP checksum validation ok.	HC
20	**FRAG.** Fragment IP datagram	HC
19	**CKSMZO.** Received packet with UDP checksum field zero	HC
18	**IPKT.** NIC received a IP packet.	HC
17	**TPKT.** NIC received a TCP packet.	HC
16	**UPKT.** NIC received a UDP packet.	HC
15:0	**PQTAG.** VID/PRI TAG[14:0].	HC

FIFO and Control Logic

The VT6130 incorporate on-chip RAM for transmission and receive data buffering from the system interface to the network interface, providing temporary storage of data, to free host system from the real-time demands on the network.

The VT6130 transmit FIFO controller has advanced adaptive traffic control mechanism to maintain a back-to-back send at wire speed

The VT6130 has enhanced Receive FIFO management logic to handle multiple received data packets transfer to system data buffer. This ability can reduce the packets losing due to host bus latency.

Media Type and Auto-Negotiation

The VT6130 supports 10Base-T/100Base-T/1000Base-T.

The 802.3 2002 Auto-Negotiation defines automatic negotiation of signaling rate and duplex mode between two ends of a twisted pair link segment. The VT6130 supports Auto-Negotiation defined Priority Resolution Table fetched from the integrated PHY to decide current operating mode of the media port.

The VT6130 supports media port selected in different ways depending open the state of internal configuration.

Auto-Negotiated/Force Mode

Through Auto-Negotiation, the PHY attempts to negotiate a 10/100/1000 Base-T link with a remote adapter. After the negotiation process is completed, the VT6130 can decide if a link is up and the speed rate and duplex through the PHY's Auto-Negotiation registers.

Also, the VT6130 can be programmed to a desired operating speed 10/100/1000 G bps and duplex mode (FDX or HDX) through forced operation.

CAM Based Preface Filtering

The address recognition logic of VT6130 controller use Content Address Memory (CAM) technology to support unicast, multicast and interesting packets perfect filtering and VID perfect filtering for VLAN supporting.

Programming CAM

The VT6130 driver initializes CAM by enabling CAM read/write function, CAMEN = 1.

- Set CAM entry address, (CAMADD)
- Set CAM entry data
- Address_CAM: offset 10 ~ 15h, 48 bits
- VID_CAM: offset 10 ~ 11h, 12 bits
- Set CAMWR
- Wait CAMWR self clear
- Execute next CAM entry programming

Read CAM

The VT6130 driver download CAM contents by

- Enable CAM read/write function, CAMEN = 1
- Set CAM entry address (CAMADD)
- Set CAMRD
- Wait CAMRD self clear
- Tead CAM content from data port
- Address_CAM: offset 10 ~ 15h, 48 bits
- VID_CAM: offset 10 ~ 11h, 12 bits

Unicast/Multicast Perfect Filtering

Program Address_CAM with accepted Ethernet address.

Turn on the CAMMASK bits to enable related Address_CAM entries.

Turn on AM: incoming multicast packets will be filtered with perfect address

Turn on AP: incoming packets will be filtered by comparing with those active entries (CAMMASK bits enabled) defined in Address_CAM

If the number of multicast address is larger than 64, the multicast hash tables can be used also.

CAM content won't be cleared by any types of reset. We can only control the CAMMASK to handle the active entries.

Interesting Packet Perfect Filtering

Interesting packets are a group of packets with specified Multicast Address. The VT6130 provides max 32 interesting packets filtering capability. The hits index will be stored and write-back to RD status

The operation is as follows:

- Program the interesting packet address into Address_CAM
- For each incoming packet, check the RD.IPKT field to see which interesting packet received

Checksum Offload

The VT6130 provides hardware based TCP/IP. UDP/IP checksum calculation and validation. On Transmission, the host requests TCP/IP checksum offloading by setting the control bit in the transmit descriptor (TD) header control field. On reception, when the checksum offload enable bit is set, every packet is parsed for the presence of IP, TCP, and UDP headers. For any of those found, checksum logic will calculate and compare with those related fields in the packet. Any mismatches will be flagged as checksum error and the status is kept at write back status field and is transferred to the host by normal packet reception write back flow.

VT6130 checksum offload feature supports IPV4 only, packets of other IP version will be ignored.

IP forms are EtherType=0800h, IEEE 802.2 and SNAP.

Fragmented IP datagrams are not supported

IEEE 802.1q Compliant VLANs

VLAN

The VT6130 supports IEEE 802.1q Virtual Local Area Network (VLAN). In a VLAN environment, the controller will respond to range of 64 individual address. Allowing multiple VLAN support.

IEEE 802.1q VLANs

802.1q frames have 4 extra bytes over normal 802.3 frame format. Two of the 4 bytes contain a special type (TPID) and the other two bytes contain 12 bit VLAN ID number, 3 bits of priority and a “token Ring encapsulation” bit. The VT6130 adapter will take an oversized frame on a 802.1q packet if it is larger than MaxPktSize+4.

With frame tagging, each VT6130 can support up to 64 IP address assignments on a single network connection, allowing servers to be accessed from systems in multiple IP subnets without traversing routers. It also allows users to define multiple application VLANs to partition traffic for performance and security purpose.

In summary, the VT6130 support Multiple Virtual LAN (VLAN)

Long frame support (1518+4) bytes

- VLAN tag insertion for transmit packets
- VLAN tag detection and removal for receive packets
- VLAN status could be written back to the Receive Descriptor

IEEE 802.1p Priority Transmit

To meet current Multi-Media application and maintain the Quality Of Service (QOs), VT6130 supports IEEE 802.1p and provides 4 levels of priority. The priority DMA scheduler maintains flexible queuing usage depends on driver’s setting. The VT6130 hardware and software maintain 4 TD queues in advanced priority DMA scheduler, and also provide non-blocking mode for high performance application requirement.

Flow Control

The VT6130 supports half duplex Jam based and IEEE 802.3x flow control scheme while in full duplex.

When VT6130 detects the system is busy and receive buffers or the internal FIFO are running up,

In half duplex mode, MAC will send jam pattern automatically, when addressed packets coming to stop the transmission from source station.

In full duplex mode, VT6130 will generate PAUSE control frame to inform the source station to stop transmission for specified period of time defined in the PAUSE frame. After the busy condition is clear, VT6130 will send another PAUSE control frame with pause_time (0000h) to inform the source station of getting ready to receive packets.

VT6130 also implements detection logic to filter coming pause control frame, when a valid PAUSE control frame is detected, VT6130 will enter backoff state after current transmission completed and wait for the specified period of time defined in the received PAUSE frame. VT6130 will re-transmit other packets in transmit queue after receiving a new pause frame with pause_time (-0000h) or when the pause timer is expired. Also, the IEEE 802.3x flow control capability is the negotiated results form N-way and can be optionally disabled.

Chip Configuration EEPROM Contents

Offset ID	Bit[15:8]	Bit[7:0]
00h	Ether ID1	Ether ID0
01h	Ether ID3	Ether ID2
02h	Ether ID5	Ether ID4
03h	SW_Reserved	(G)MII PHYID
04h	SUB_SID1	SUB_SID0
05h	SUB_VID1	SUB_VID0
06h	DevID1	DevID0
07h	VenID1	VenID0
08h	Data_SEL	PMCC
09h	AuxCurr	PMU_DATA_REG
0Ah	MCFG1	MCFG0
0Bh	MAX_LAT*	MIN_GNT
0Ch	DCFG1	DCFG0
0Dh	CFG_B	CFG_A
0Eh	CDG_D	CFG_C
0Fh	checksum**	(73/74/83/84***h)
10h	Serial Number[15:0]	
11h	Serial Number[31:16]	
12h	Serial Number[47:32]	
13h	Serial Number[63:48]	

Note:
1.
* Word 0Bh to 0Eh can be modified by embedded programming
** EEPROM CONTENTS CHECK SUM DEFAUT=<55>h at offset 93h
*** (73/74) h = EEPROM programmed status
*** (83/84) h = EEPROM programmed status and with serial number
2. where to locate PHY ADDR for MII management port (00001) is recommended
3. 10h ~ 13h will be load if the serial number capability is support
3. Read /load sequence = 06-07-04-05-08-09-00-01-02-03-0A-0B-0C-0D-0E-0F-10-11-12-13

Power Management

The VT6130 is compliant to ACPI v1.0, PCI Power Management v1.1 and Network device class power management v1.0a. It meets PC97/PC98/PC99/PC2001 and net PC requirements. When the system enters power down mode, four wake-up events are supported in VT6130 and can wake up the system via WAKE# or BEACON to restore to running state to process normal jobs when wake up events are detected.

Wake On LAN

The VT6130 can be configured to support remote wake up by defined wake up events in every PCI Express PME defined power states via WAKE# or BEACON indication. Also a Magic packet scheme. Wake up at PCIe power abnormal shut down or AC power loss by remote Wake On LAN management station.

Wake Up Events

- **Link Status Change**: If this link stat have changed connect or disconnected, WAKE# or BEACON will be generated when link state change.
- **Magic Packet**: When VT6130 is set to magic packet mode, it requires that a received packet qualify as a Magic Packet
- **Magic Packet Pattern**: The Magic packet pattern 6 FFh byte + SA duplication 16 times destination address of received magic packet matches, meanwhile Magic register (RxA0[5]) set enable, VT6130 will received this packet.
- **Unicast Physical Address Match**: When VT6130 is set to unicast mode, it require that a received packet qualify as a unique individual address and unicast register bit (RxA0[5]) set enable, VT6130 will receive this packet.
- **MS Defined Pattern Match**: When the stations shutdown after operation system is loaded, the IP address station name or other defined value are set by the drivers to VT6130 define 8 (or 16) sets of interesting pattern match

PMU Capability Related SR: (08Lo)

PMCC	DSI	D2_Dis	D1_Dis	D3C_EN	D3H_EN	D2_EN	D1_EN	D0_EN
DATSEL		EN	Data_scale		Data_Sel			
AuxCurr						AuxCur[2]	AuxCur[1]	AuxCur[0]

Note:
1. EN indicates if DataReg implemented completely.
   0: Data_Sel will be read only, and PMU DATAREG will be 8'h00 always.
   1: Data_Sel can be written update.
2. In 65c, the PMU Data Register won't be implemented completely. The EN bit should be 0 in EEPROM in all application.

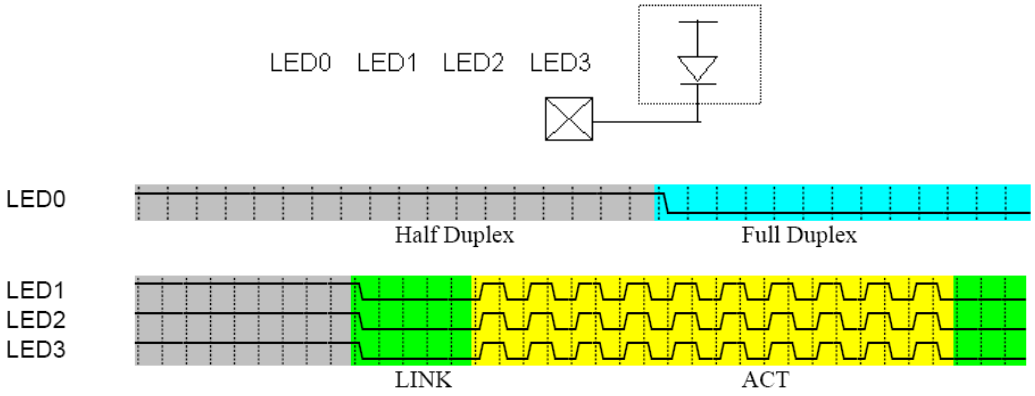
Medium Dependent Interface (MDI) for Twisted Pair Cable

The interface between VT6130 and CAT5 cable consists of four signal pairs, channel A, B, C, and D, that are used for 1000BASE-T transmission/receiving. Each signal pair consists of two bi-directional pins that transmit and receive data stream at the same time.

When the VT6130 operates in 100BASE-TX or 10BASE-T mode, only channel A and B are used. One is for transmission; the other is for receiving. VT6130 will handle the MDIX/MDI crossover issue of the twisted-pair wire automatically. Please refer to *Auto MDI/MDIX Crossover* for details.

LED Interface

4 status LEDs with 4 programmable modes to communicate its operating conditions (Duplex, 10 Link/ACT, 100 Link/ACT, 1000 Link/ACT). In LOM (Lan On Motherboard) applications, the most popular configuration is using one RJ-45 jack with 2 glued LEDs. One of them is built with single light and the other one is built with dual lights. As following diagrams show:



Note: In LED1 / LED2 / LED3, only one pin active at the same time.

Figure 3. Case 0

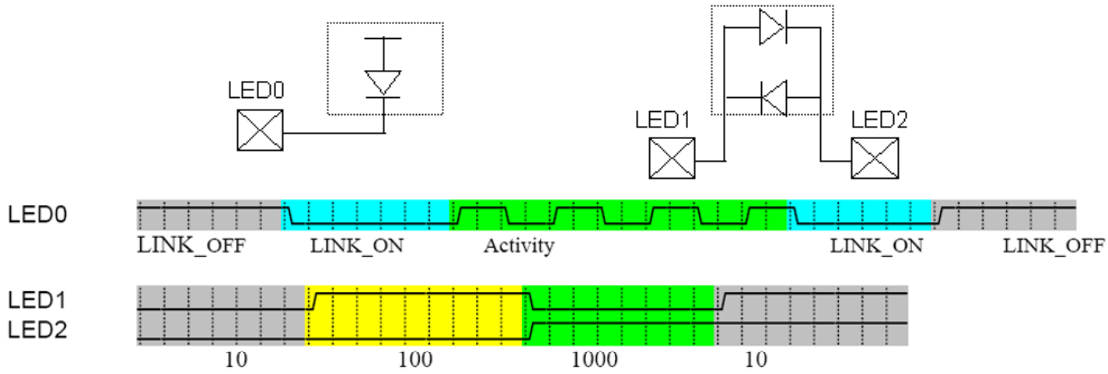
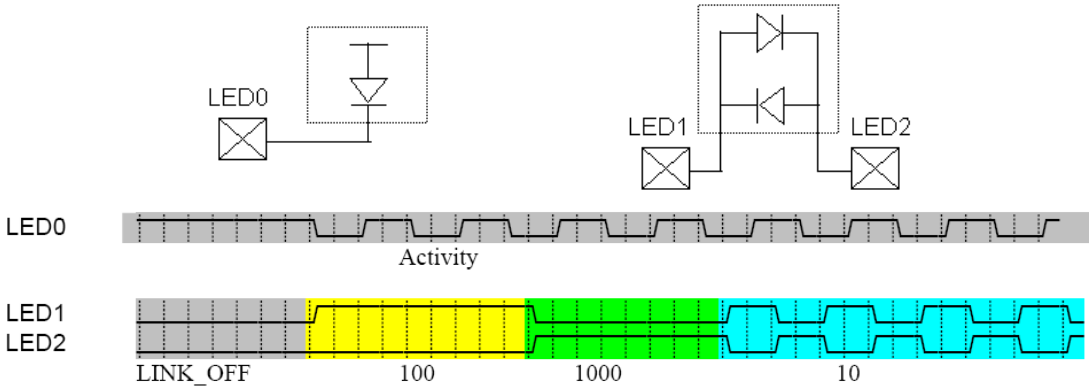


Figure 4. Case 1



Note: LED2 and LED3 oscillate in 10Hz to have light mixed.

Figure 5. Case 2

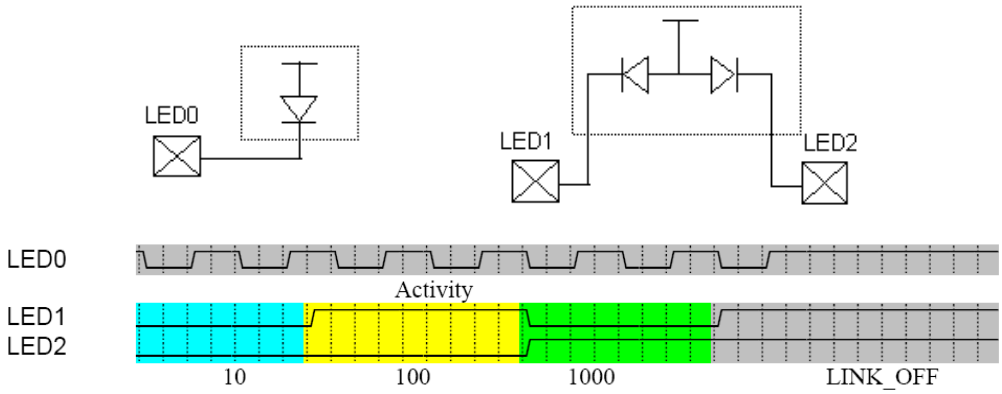


Figure 6. Case 3

LED Control Specification

Table 9. LED Select

LEDS1, LEDS0	LED0	LED1	LED2	LED3
00	Duplex	10 Link/ACT	100 Link/ACT	1000 Link/ACT
01	CASE_1			
10	CASE_2			
11	CASE_3			

LED Dark Function

VT6130 also supports LED dark function. It will advance to reduce power consumption for some specific application. Following is the control table.

LED_PCIVF	LED_OFF	PCI 5V	LED
0/1	1	0/1	Dark
0	0	0/1	case0/case1/case2/case3
1	0	1	case0/case1/case2/case3
1	0	0	Dark

LED_PCIVF (0x78[6]): located at suspend well. SW programmable in D0 and loaded from EEPROM, reset value is 0.

LED_OFF (0xA3[6]): located at suspend well, SW programmable, reset value is 0.

Auto MDI/MDIX Crossover

The VT6130 implements auto-crossover function; i.e. users don't have to care using a crossover or non-crossover cable. Its pin mapping in MDI/MDIX modes is shown in the following table. If VT6130 interoperates with a device that does not implement auto MDI/MDIX crossover, the VT6130 makes the necessary adjustment prior to performing auto-negotiation. If the VT6130 interoperates with a device that implements auto MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 section 40.4.4 determines which device performs the crossover.

When the VT6130 interoperates with a 10BASE-T PHY or a PHY that implements auto-negotiation, it decides the MDI/MDIX by the present of link pulse, however, when interoperating with a 100BASE-TX PHY that does not implement auto-negotiation (i.e. link pulses are not present), VT6130 uses signal energy of receiving MLT3 signals to determine whether or not to crossover.

The auto MDI/MDIX function is turned on automatically after hardware reset and users can disable it by programming MII register 20.2. Users can check if VT6130 is in MDI/MDIX type by reading MII offset 11[11]. Auto MDI/MDIX function is not affected by disabling auto-negotiation function.

Pin	MDI			MDIX		
	1000BASE-T	**100BASE-TX**	**10BASE-T**	**1000BASE-T**	**100BASE-TX**	**10BASE-T**
MDI[0]P/M	BI_DA+/-	TX+/-	TX+/-	BI_DB+/-	RX+/-	RX+/-
MDI[1]P/M	BI_DB+/-	RX+/-	RX+/-	BI_DA+/-	TX+/-	TX+/-
MDI[2]P/M	BI_DC+/-	Unused	Unused	BI_DD+/-	Unused	Unused
MDI[3]P/M	BI_DD+/-	Unused	Unused	BI_DC+/-	Unused	Unused

Polarity Correction

The VT6130 performs polarity correction without any manually setting. It corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes automatically.

In 1000BASE-T mode, polarity correction is based on the sequence of idle symbols. In 10BASE-T mode, polarity correction is based on the detection the polarity of valid normal link pulse and idle pulse. In 100BASE-TX mode, the polarity does not matter.

Auto-Negotiation

VT6130 will perform Auto-Negotiation automatically if one of the following conditions happened:

1. Power up reset, hardware reset, or software reset (by programming MII register 0.15).
2. Restart Auto-Negotiation (by programming MII register 0.9).
3. Transition from power down to power up (by programming MII register 0.11).
4. Link is down.

Once Auto-Negotiation is initiated, VT6130 sends out the appropriate base pages/ next pages to advertise its capability and negotiate with the link partner to determine speed, duplex, and master/slave. Note that VT6130 handles the base page/ next page exchanges automatically without user intervention. To link at giga mode, the link partner of VT6130 has to support Auto-Negotiation, too. Once VT6130 completes Auto-Negotiation it updates the statuses in registers 1, 5, 6, 10 and 17. The advertised abilities can be changed by writing registers 4 and 9. It is noted that a write access to register 4 or 9 has no effect once the VT6130 begins transmitting Fast Link Pulses (FLPs). This guarantees that the transmitted FLPs are consistent. Register 7 is treated in a similar way as registers 4 and 9 during additional next page exchanges

If the link partner doesn't support Auto-Negotiation, VT6130 determines the link speed using parallel detection and the link result is either 10M half or 100M half. Please refer to IEEE 802.3 clause 28 and 40 for more detail description of Auto-Negotiation.

Auto-Negotiation can be disabled by programming register 0.12. When Auto-Negotiation is disabled, the speed and duplex of VT6130 can be changed by programming registers 0.13, 0.6 and 0.8 respectively.

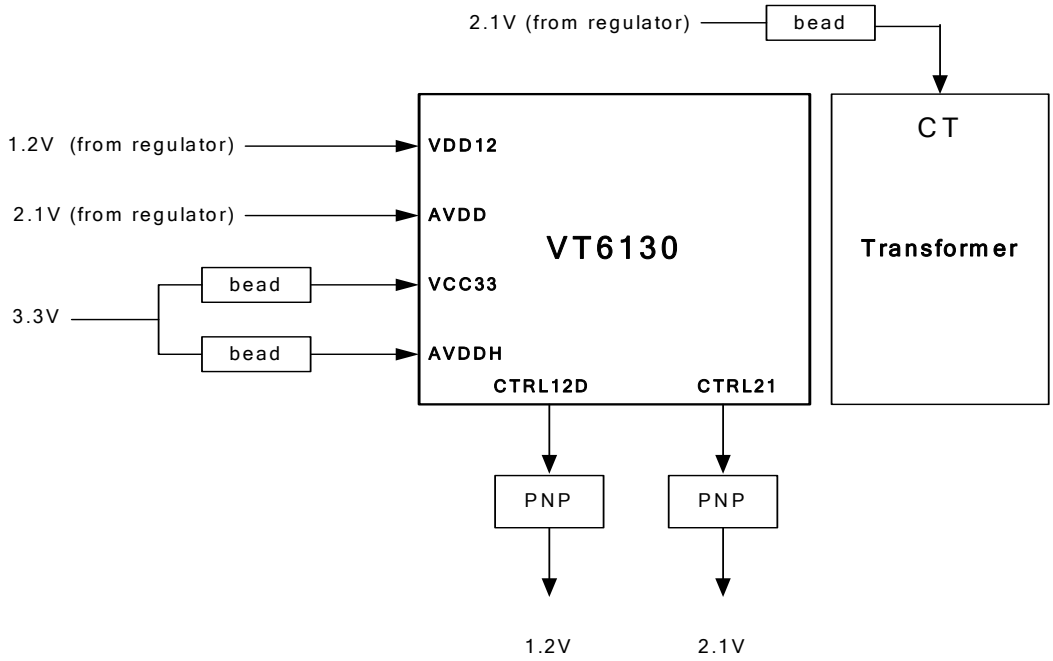
Smart Speed

VT6130 supports smart speed function. If VT6130 can't link at giga mode due to cable quality, the link speed is down shift to 100M automatically if smart speed option is turned on. If the function is turned off, VT6130 will link down if it can't link at giga mode due to cable quality. The function is default on, and it can be enabled or disabled by programming MII register 16.11.

Power Supply

VT6130 has 4 sets of power pins, VDD12, AVDD, VCC33 and AVDDH. VCC33 is connected to 3.3V. AVDDH can use the same power source of VCC33, but it needs a bead to prevent noise from VCC33. AVDD can be connected to 2.1V. Users can use the 2.1V power generated by the built-in regulator (CTRL21).

VDD12 is connected to 1.2V. The center tap of transformer can be connected to 2.1V. Users can use the 2.1V power generated by the built-in regulator (CTRL21).



Digital Communication Internal Function

The VT6130 integrates all necessary function blocks to achieve the communication ability over CAT5 unshielded twisted pair cables. These function blocks include analog blocks and digital blocks.
Analog function blocks includes analog to digital converter (ADC), digital to analog converter (DAC), active hybrid, and high-speed 1.25GHz transmitter/receiver. Digital function blocks include digital adaptive feed-forward equalizer (FFE), decision-feedback equalizer (DFE), echo canceller (EC), near-end-cross-talk canceller, baseline wander canceller, and digital phase lock-loop (DPLL). Some other encoding/decoding blocks are also necessary in the transmission/receiving data path.

Statistics (MIB Operation)

Index (Hex)	Description
00	**RxAllPkts**. The total number of packets (including bad packets, broadcast packets, and multicast packets) received. 1. If receive mode affect the result (AR,AM,AB,AU) 2. Implementation: Those incoming packets with DA match.
01	**RxOkPkts**. 1. The number of incoming frames that are successfully received. 2. It depends on the receive mode setting (AR, AB, AM, AU, AL) 3. Implementation: RxOkPkt
02	**TxOkPkts.** The count of the number of frames that are successfully transmitted.
03	**RxErrorPkts**. 1. Frames Lost Due to Receive Errors is a count of the number of frames that should have been received (the DA matched) but experienced a receive FIFO overrun error. 2. Only includes overruns that become apparent to the host system, and does not include frames that are completely ignored due to a completely full rxfifo at the beginning of frame reception.*(in fact, only RACEI, no OVFI)* 3. Implementation: FOVF+ RACE + RDERR
04	**RxRuntOkPkt**. 1. Controlled by AR (AU/AM/AB) 2. Packet size < 64 and well formed 3. Implementation: Accepted Runt Packet (good CRC)
05	**RxRuntErrPkt**. 1. It counts both runts and noise hits. 2. Implementation: (pkt < 64) & (CRCE|FAE)
06	**Rx64Pkts**. 1. Counting the incoming packet byte include 802.1p/q tag regardless of whether the tag removing or not. 2. Including error packet 3. Implementation
07	**Tx64Pkts**. 1. Number of packet with 64octets transmitted
08	**Rx65To127Pkts.**
09	**Tx65To127Pkts**
0A	**Rx128To255Pkts**
0B	**Tx128To255Pkts**
0C	**Rx256To511Pkts**
0D	**Tx256To511Pkts**
0E	**Rx512To1023Pkts**
0F	**Tx512To1023Pkts**
10	**Rx1024To1518Pkts**
11	**Tx1024To1518Pkts**
12	**TxEtherCollisions** 1. The total number of collision on Ethernet segment. 2. Implementation: TxCollCnt
13	**RxPktCRCE** 1. Implementation: CRCE
14	**RxJumboPkts** 1. Criteria: Jumbo Packet definition 2. Implementation: RcvJumboPkt
15	**TxJumboPkts** 1. Implementation: TxmitJumboPkt
16	**RxMacControlFrames** 1. The number or MAC control PAUSE frames, and only PAUSE frames, received successfully. 2. Implementation: RxPauseFrames
17	**TxMacControlFrames** 1. The count of MAC control frames transmitted. 2. Not include the frame transmitted by host. 3. Implementation: TxPauseFrames
18	**RxPktFAE** 1. Implementation: FAE
19	**RxLongOkPkt** 1. Provide *MaxFrameSize* for threshold control.(including 802.1P/Q Tag option) 2. Implementation: Accepted Long Packet (over MaxFrameSize

1A	**RxLongPktErrPkt** 1. Consider 802.1p/q tag packet case 2. Implementation: (pkt > MaxFrameSize) & (CRCE|FAE)
1B	**TXSQEErrors** 1. Loss of collision heartbeat during transmission. 2. Implementation: SQE
1C	**RxNobuf** 1. Implementation: the Rx lost packet count caused by Nobuf. LSTEND_1: receive packet nobuf RBUFF: receive packet linking without Rx buffer.
1D	**RxSymbolErrors** 1. Be care the GMII RXER cases. 2. Implementation: RXER
1E	**InRangeLenthErrors** 1. 64 <= PktLen <= 1518 2. Implementation: RxLenErr
1F	**LateCollisions** 1. Late Collisions is a count of the number of times that a collision has been detected later than 1 slot time into the transmitted frame. 2. Be care the late-collision window in GMII. 3. Implementation: LateColl

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_S	Storage Temperature	-55	—	125	°C
T_A	Ambient Operating Temperature	0	—	70	°C
V_{CC}	3.3V I/O Supply Voltage	V_{CC} - 0.33	3.3	V_{CC} + 0.33	V
V_{DD}	1.2V Core Voltage	V_{DD} - 0.12	1.2	V_{DD} + 0.12	V
V_{DDA}	2.1V Analog Part Voltage	V_{DDA} - 0.21	2.1	V_{DDA} + 0.21	V
V_{DDRAM}	1.2V Internal SRAM Voltage	V_{DDRAM} - 0.12	1.2	V_{DDRAM} + 0.12	V
—	ESD HBM Rating	—	—	±2500	V

Note: **Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.**

DC Specifications

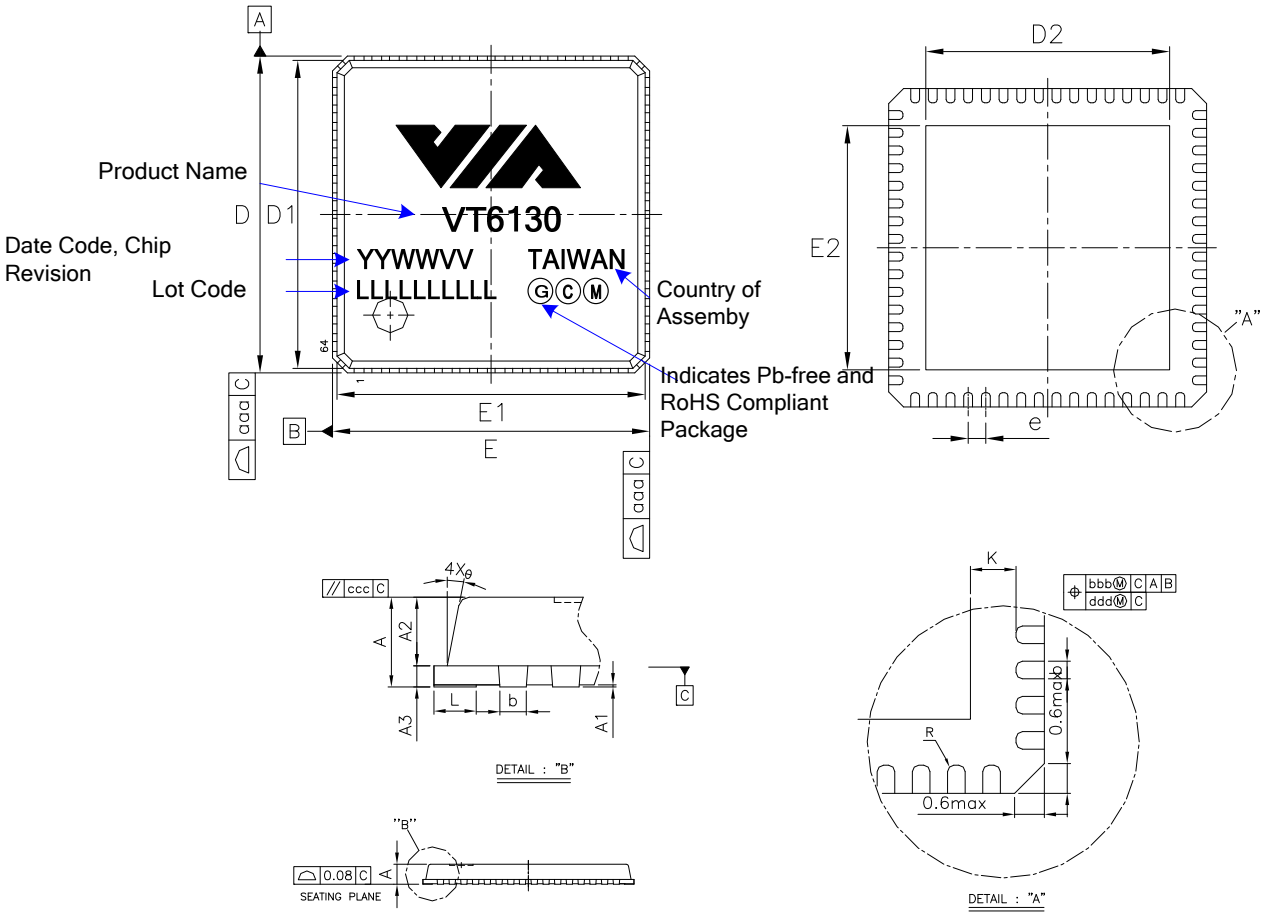
T_A = 0-70° C, V_{DD} = V_{DDRAM} = 1.2V±5%, V_{DDA} = 2.1V±5%, V_{CC} = 3.3V±5%, GND = 0V

Table 11. DC Specifications

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IL}	Input Low Voltage	-0.5	0.8	V	—
V_{IH}	Input High Voltage	2.0	VCC+0.3	V	—
V_{OL}	Output Low Voltage	—	0.45	V	I_{OL}= 4.0 mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH}= -1.0 mA
I_{IL}	Input Leakage Current	—	±10	uA	0< V_{IN} < V_{CC}
I_{OZ}	Tristate Leakage Current	—	±20	uA	0.45 < V_{OUT} < V_{CC}

Note: **These parameters are not guaranteed by production testing, All electrical specifications are based on IEEE 802.3 requirements and internal design considerations.**

MECHANICAL SPECIFICATIONS



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3		0.20 REF			0.008 REF	
b	0.23	0.25	0.28	0.009	0.010	0.011
D		9.00 BSC			0.354 BSC	
D1		8.75 BSC			0.344 BSC	
D2	6.75	6.90	7.05	0.266	0.272	0.278
E		9.00 BSC			0.354 BSC	
E		8.75 BSC			0.344 BSC	
E2	6.75	6.90	7.05	0.266	0.272	0.278
e		0.50 BSC			0.020 BSC	
L	0.35	0.40	0.45	0.014	0.016	0.018
θ	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
chamfer	---	---	0.60	---	---	0.024

Figure 7. QFN-64 Package (9 × 9 mm)