Data Sheet

VT1625 and VT1625M
HDTV Encoder

Preliminary Revision 1.0
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VIA TECHNOLOGIES, INC.

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PRODUCT FEATURES

- **Input Format**
  - Digital RGB 24/30-bit color input video data in both interlace and non-interlace formats with 12/15-bit multiplexed input data path depth
  - Digital RGB 15/16/18-bit color input video data in both interlaced and non- interlaced formats with 8-bit multiplexed or 15/16/18-bit non-multiplexed input data path depth
  - Digital YCrCb 8/10 or 16/20-bit 4:2:2 (CCIR656 or CCIR601) input video data in both interlace and non-interlace formats with 16-bit multiplexed or 20-bit none-multiplexed input data path depth
  - Digital YCrCb 8/10 or 16/20-bit 4:2:2 HDTV input video format (BT709, BT1120, SMPTE274M) in both interlace and non-interlace formats with 16-bit multiplexed or 20-bit non-multiplexed input data path depth.
  - Digital YCrCb 24/30-bit 4:4:4 color input data in both interlace and non-interlace formats with 12/15-bit multiplexed input data path depth
  - Flexible pixel ordering with various alternate formats (Please check the Input Data Format table for more detail)
- **Output Format**
  - Compliant with NTSC (M and J) or PAL (B, D, G, H, I, M, N and Nc) TV system
  - Composite, S-Video, Component (YPbPr), Analog RGB (SCART) with interlaced or non-interlaced scan output
  - Component (YPbPr) and Analog RGB (SCART) with progressive scan output
  - SDTV output mode (525p or 625p) compliant with EIA770-1 and EIA770-2
  - HDTV support for 1080i (D3) and 720p (D4) compliant with EIA770-1, EIA770-2, EIA770-3 and ITU-RBT 709-4
  - Output resolution support NTSC - 525i(480i), 525p(480p), PAL - 625i(576i), 625p(576p), HDTV - 1080i, 720p
  - D-Terminal support from D1 ~ D4 stage
  - 85 MHz VGA DAC for secondary VGA Monitor
- **High Quality 6x10-Bit Video DAC**
  - Simultaneous Composite + S-Video + Component (YPbPr) outputs display
  - Simultaneous Composite + S-Video +RGB (SCART) outputs display
  - Simultaneous Component (YPbPr) + RGB (SCART) outputs display
  - Six flexible and programmable DACs for each specific video signal output
- **Macrovision (VT1625M Only)**
  - Macrovision™ 7.1.L1 copy protection support
  - Macrovision™ 1.2 AGC copy protection with 525p / 625p progressive scan output
- **Other Features**
  - Input from graphics resolution 640x480 to 1024x768, 1280x720p, 1920x1080i, 1920x1080p
  - VIA Advance ProScale™ Technology for HDTV standard output, input resolution can be 640x480 ~ 1024x768 --> 1080i, 720p standard HDTV resolution
  - Studio grade encoder
  - HDTV tri-level synchronization and broad pulse insertion
  - Separate adjustable Y U V delay
  - Programmable 2D scaling
  - Adaptive deflicker filter to enhance TV image quality
  - Programmable sharpness / adaptive filter control
  - Support for CGMS-A / Wide Screen Signaling (WSS) / Closed Captioning for variable clock rates adheres to EIAJ-1204, 1204-1, 1204-2 and EN 300 294 standards.

- Standard CCIR656 format output
- Three general purpose output ports
- Multiple Chroma and Luma filters
- P:P2 clocking mode or fixed clock mode for full TV screen
- Automatic detection of TV presence
- Programmable power save management
- Master, slave and pseudo master video timing operation
- Serial bus programming interface
- Hot plug interrupt support
- Variable I/O voltage interface (1.0 ~3.3V) to graphic device
- DAC auto adjustment
- TSMC advance 0.22um low power CMOS process, 2.5V core power
- 64-pins TQFP package (10 x 10 x 1.0mm)

OVERVIEW

The VT1625 and VT1625M are digital High Definition Television encoders that accept various RGB pixel data formats or the YCrCb (compatible with CCIR656 or CCIR601) pixel data format from the graphic chip or the MPEG decoder. It is designed to support any input resolution from 640x480 to 1024x768, including the HDTV input format 1280x720 or 1920x1080. It is capable of performing non-interlace to interlace conversion to generate high-quality flicker-free video signals. It supports the following video signal formats: Composite video, S-Video, RGB (SCART), Component (YPrPb), and interlaced or progressive scan output signals for NTSC-525i(480i), 525p(480p), PAL-625i(576i), 625p(576p), HDTV-1080i, 720p and D-Terminal (D1 to D4).

The ASIC uses VIA Advance ProScale™ Technology which can scale the input resolution as 640x480 ~ 1024x768 encode for 1080i, 720p standard HDTV resolution output. The newest VIA ProScale® engine provides the most advanced vertical and horizontal scaling technology. Using the programmable CRTC and the scaling factor, the ASIC can scale an image from 0.5 to 1.5 factors in the horizontal / vertical directions. It uses an adaptive deflicker filter that checks the graphics on a pixel-by-pixel basis to maintain a flicker-free display.

The TV encoder is capable of supporting various worldwide video standards, including NTSC-M (North America, Taiwan), NTSC-J (Japan), PAL-B, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay) and PAL-Nc (Argentina). Since there are six DACs they can be programmed into specific video signal outputs for Composite, S-Video (Y/C), Component (YPrPb), RGB (SCART). They can simultaneously output composite video, S-Video, component, RGB signals with interlace/non-interlace scan mode, or output an analog progressive scan signal in YPbPr or RGB format. The video DACs can also be programmed for CRT RGB DAC (85MHz) to display secondary CRT monitor.

In addition, the VT1625M can output video with the Macrovision 7.1.L1 anticopy video signal or the Macrovision 1.2 AGC copy protection with 525p and 625p progressive scan output. The Macrovision anticopy process provides a means to deter the unauthorized copying of copy protected analog video signals onto videocassettes.

All features are software programmable through a serial bus interface that provides read / write access to all registers.

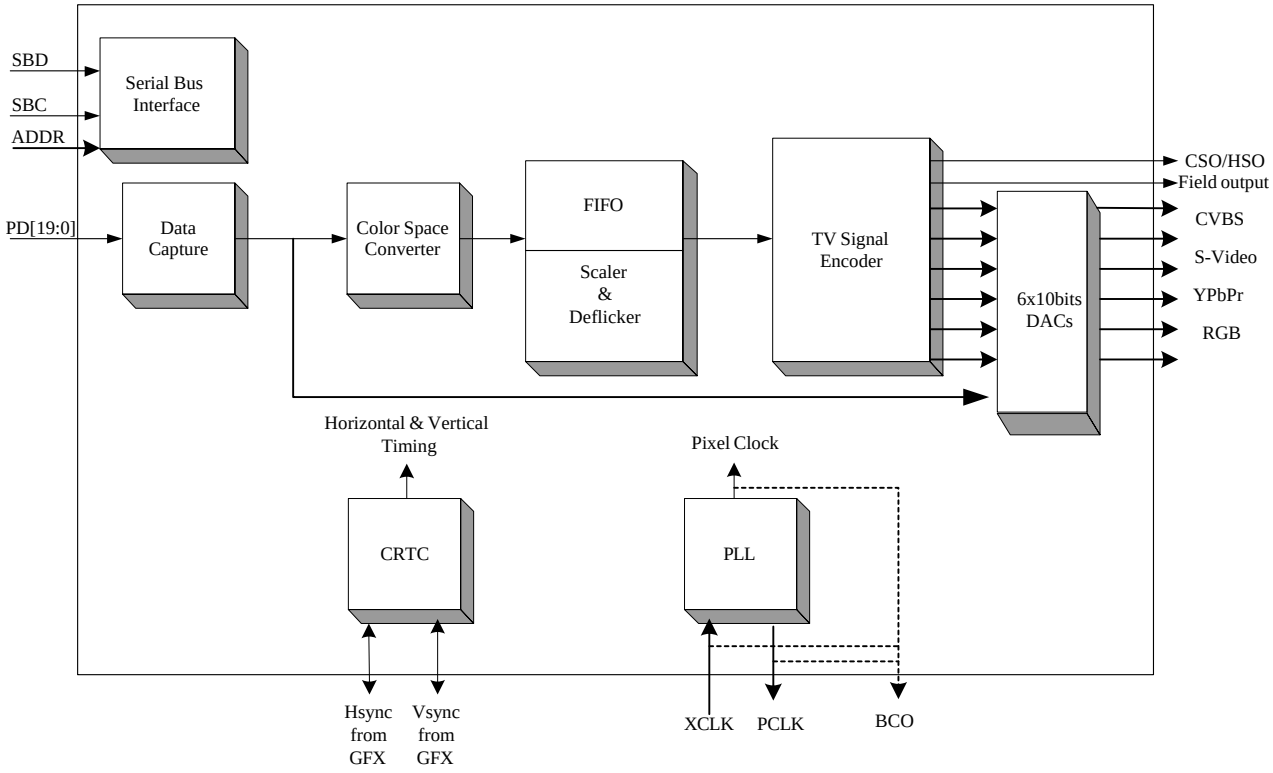


Figure 1. Functional Block Diagram

PINOUTS

Pin Diagram

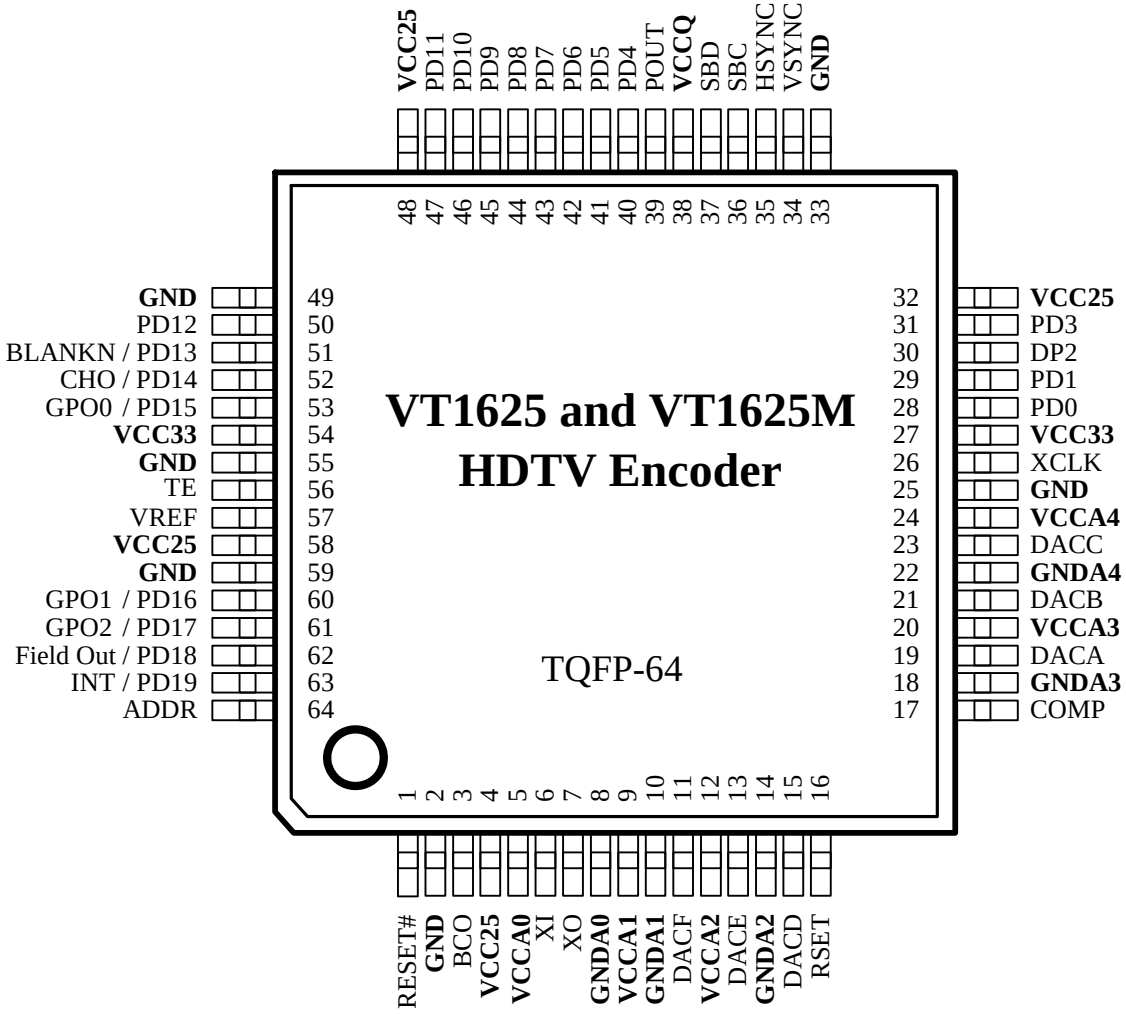


Figure 2. Pin Diagram (Top View)

Pin List

Table 1. Pin List (Alphabetical Order)

Pin	Type	Pin Name	Pin	Type	Pin Name
64	I	ADDR	41	I	PD5
3	O	BCO	42	I	PD6
52	I/O	CHO / PD14	43	I	PD7
53	I/O	GPO 0 / PD15	44	I	PD8
17	I	COMP	45	I	PD9
19	O	DACA	46	I	PD10
21	O	DACB	47	I	PD11
23	O	DACC	50	I	PD12
15	O	DACD	51	I	BLANKN / PD13
13	O	DACE	39	O	POUT
11	O	DACF	1	I	RESET#
60	I/O	GPO 1 / PD16	16	I	RSET
8	**P**	**GNDA0**	36	I	SBC
10	**P**	**GNDA1**	37	I/O	SBD
14	**P**	**GNDA2**	56	I	TE
18	**P**	**GNDA3**	**5**	**P**	**VCCA0**
22	**P**	**GNDA4**	**9**	**P**	**VCCA1**
61	I	GPO 2 / PD17	**12**	**P**	**VCCA2**
62	I	Field out / PD18	**20**	**P**	**VCCA3**
35	I/O	HSYNC	**24**	**P**	**VCCA4**
63	I	INT / PD19	**38**	**P**	**VCCQ**
28	I	PD0	54	I	VREF
29	I	PD1	34	I/O	VSYNC
30	I	PD2	26	I	XCLK
31	I	PD3	6	I	XI
40	I	PD4	7	O	XO

VCC25 (4 pins): 4, 32, 48, 58
VCC33 (2 pins): 27, 54
GND (6 pins): 2, 25, 33, 49, 55, 59

Pin Descriptions

Table 2. Pin Descriptions

Pixel Data In			
Signal Name	**Pin #**	**Type**	**Description**
PD19 / INT **PD18** / Field out **PD17 /** GPO 2 **PD16** / GPO 1 **PD15 /** GPO 0 **PD14 /** CHO **PD13 /** BLANKN **PD[12:0]**	63 62 61 60 53 52 51 50,47-40,31-28	I	**Pixel Data In.** These inputs can accept 8, 12, or 16 bit multiplexed or non-multiplexed digital RGB or YCbCr format video stream. PD13 ~ PD19 are multi-function pins.
HSYNC	35	I/O	**Horizontal Sync.** When the HSYO bit (Rx01[2]) is low, this pin can accept a horizontal sync input. When the HSYO bit is high, the device will output a horizontal sync pulse through this pin.
VSYNC	34	I/O	**Vertical Sync.** When the VSYO bit (Rx01[3]) is low, this pin can accept a vertical sync input. When the VSYO bit is high, the device will output a vertical sync pulse through this pin.

Control Pins			
Signal Name	**Pin #**	**Type**	**Description**
VREF	57	I	**Voltage Reference. Typical VREF = ½ VCCQ** This is reference voltage level for I/O interface (data, sync)
BLANKN / PD13	51	I	**Input for Display Blank**. The rising edge of this signal identifies the first blank pixel of data for each blank line.
Field Out / PD18	62	O	**Field Output.**

TV Output			
Signal Name	**Pin #**	**Type**	**Description**
CHO / PD14	52	I	**TV Composite Sync / Horizontal Sync output,** **VGA HSYNC output (VGA bypass mode)**
INT / PD19	63	I/O	**TV Sense Hot Plug Interrupt.**
GPO 0 / PD15	53	O	**General Purpose Output 0.**
GPO 1 / PD16	60	O	**General Purpose Output 1.**
GPO 2 / PD17	61	O	**General Purpose Output 2.**
DACA	19	O	**DAC A Analog Output.**
DACB	21	O	**DAC B Analog Output.**
DACC	23	O	**DAC C Analog Output.**
DACD	15	O	**DAC D Analog Output.**
DACE	13	O	**DAC E Analog Output.**
DACF	11	O	**DAC F Analog Output.**

Serial Bus Interface			
Signal Name	**Pin #**	**Type**	**Description**
SBC	36	I	**Serial Bus Clock.** This pin acts as the clock pin of the serial bus interface and operates with inputs from 0 to VCC.
SBD	37	I/O	**Serial Bus Data.** This pin acts as the bi-directional data pin of the serial bus interface and operates with inputs from 0 to VCC. Outputs are driven from 0 to VCC.
ADDR	64	I	**Serial Bus Address Select. Low for 40h, High for 42h.**

Clock, Reset and Test			
Signal Name	**Pin #**	**Type**	**Description**
BCO	3	O	**Buffered Clock Output or TV Vertical Sync,** **VGA VSYNC (VGA bypass mode)** Provides a buffered clock output, program the Rx1E[6-4] for output select.
POUT	39	O	**Pixel Clock Output.** This pin provides a pixel clock signal to the VGA controller. The output can operate on a 1x or 2x pixel clock frequency.
XCLK	26	I	**Input Clock.** This pin is used for reference clock by PDs. It can operate on 1x or 2x pixel clock.
TE	56	I	**Test ATPG Mode Enable.**
RESET#	1	I	**Reset.** When this pin is low, the device is held in the power-on reset condition.
XI	6	I	**Crystal In.** A 27 MHz (± 20 ppm) crystal is attached between XI and XO. An oscillator can also connected to this pin.
XO	7	O	**Crystal Out.** A 27 MHz (± 20 ppm) crystal is attached between XI and XO. If an external oscillator is attached with XI, this pin should be connected to ground.
RSET	16	I	**External Resistor**. An external resistor 4.42KΩ is connected to this pin and ground to adjust the full-scale voltage for DAC A-F.
COMP	17	I	**Compensation Capacitor.** A capacitor is connected between this pin and ground to compensate DACs.

Power and Ground			
Signal Name	**Pin #**	**Type**	**Description**
VCC25	4, 32, 48, 58	**P**	**Core Power.** 2.5V ±5%
GND	2, 33, 49, 59	**P**	**Digital Ground.** Connect to primary PCB ground plane.
VCCA0	5	**P**	**Oscillator PLL Power**. 2.5V ±5%
GNDA0	8	**P**	**Oscillator PLL Ground.**
VCCA1	9	**P**	**DAC Bandgap Power.** 2.5V ±5%
GNDA1	10	**P**	**DAC Bandgap Ground.**
VCCA2	12	**P**	**DAC Bandgap Power**. 2.5V ±5%
GNDA2	14	**P**	**DAC Bandgap Ground**
VCCA3	20	**P**	**DAC Bandgap Power**. 2.5V ±5%
GNDA3	18	**P**	**DAC Bandgap Ground.**
VCCA4	24	**P**	**DAC Bandgap Power**. 2.5V ±5%
GNDA4	22	**P**	**DAC Bandgap Ground.**
VCC33	27, 54	**P**	**I/O Power.** 3.3V
GND	25, 55	**P**	**I/O Ground.**
VCCQ	38	**P**	**I/O interface Power Level.** Can be provided by graphic controller or tied externally to the maximum voltage seen by the I/O port (Data, Sync). The normal range is 1.0V to 3.3V.

REGISTERS

Register Overview

The following tables summarize all on-chip registers. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 3. Register Summary

Offset	HDTV Encoder Registers	Default	Acc
00	Input Selection	00	RW
01	Sync Selection 0	00	RW
02	Sync Selection 1	00	RW
03	Filter Selection	00	RW
04	Output Mode	00	RW
05	Clock Control	00	RW
06	Overflow	00	RW
07	Start Active Video	00	RW
08	Start Horizontal Position	00	RW
09	Start Vertical Position	00	RW
0A	Cr Amplitude Factor	00	RW
0B	Black Level	00	RW
0C	Y Amplitude Factor	00	RW
0D	Cb Amplitude Factor	00	RW
0E	Power Management	00	RW
0F	Status Register	00	RO
10	Hue Adjustment	00	RW
11	Overflow and Misc	00	RW
12	PLL P2 Value	00	RW
13	PLL D Value	00	RW
14	PLL N Value	00	RW
15	PLL Overflow	00	RW
16	Sub-carrier Value 0	00	RW
17	Sub-carrier Value 1	00	RW
18	Sub-carrier Value 2	00	RW
19	Sub-carrier Value 3	00	RW
1B	Version ID	50	RO
1C	Overflow	00	RW
1D	Test 0	00	RW
1E	Test 1	00	RW
1F	Filter Switch	00	RW

Offset	HDTV Encoder Registers	Default	Acc
20	TV Sync Step	00	RW
21	TV Burst Envelope Step	00	RW
22	TV Sub-carrier Phase Adjustment	00	RW
23	TV Blank Level	00	RW
24	TV Signal Overflow	00	RW
4A	DAC A/B/C/D Selection	00	RW
4B	DAC F/E Selection	00	RW
4C	GPO, Undershoot and Coring Selection	00	RW
4D	Internal Color Bar and Luma Delay	00	RW
4E	UV Delay Control	00	RW
4F	Burst Maximum Amplitude	00	RW
50	Graphic Horizontal Total Pixels	00	RW
51	Graphic Horizontal Active Pixels	00	RW
52	Graphic Horizontal Overflow	00	RW
53	Graphic Vertical Total Lines	00	RW
54	Graphic Vertical Overflow	00	RW
55	TV Horizontal Total Pixels	00	RW
56	TV Horizontal Active Pixels	00	RW
57	TV Horizontal Sync Width	00	RW
58	TV Horizontal Overflow	00	RW
59	TV Burst Start	00	RW
5A	TV Burst End	00	RW
5B	TV Video Start Point	00	RW
5C	TV Video End Point	00	RW
5D	TV Video Overflow	00	RW
5E	Vertical Scale Factor	00	RW
5F	Horizontal Scale Factor	00	RW

Offset	HDTV Encoder Registers	Default	Acc
60	Scaling Overflow	00	RW
61	Horizontal Blur and Scaling Overflow Register	00	RW
62	Adaptive Deflicker Threshold and Enable Signal	00	RW
63	Scaling Horizontal Total Pixels	00	RW
64	Scaling Horizontal Total Pixels Overflow	00	RW
65	PY Amplitude Factor	00	RW
66	PB Amplitude Factor	00	RW
67	PR Amplitude Factor	00	RW
68	Post Divider	00	RW
69	Auto Correction Mode Sense Data	00	RW
6A	Field Adjust	00	RW
6B	Wide Screen Signal Start Pixel	00	RW
6C	Wide Screen Signal Data 0	00	RW
6D	Wide Screen Signal Data 1	00	RW
6E	WSS Start and Data Overflow	00	RW
6F	Wide Screen Signal Sub-carrier Value 0	00	RW
70	Wide Screen Signal Sub-carrier Value 1	00	RW
71	Wide Screen Signal Sub-carrier Value 2	00	RW
72	Wide Screen Signal Amplitude	00	RW
73	Wide Screen Signal and Close Caption Control Bits	00	RW
74	Close Caption Start Pixel	00	RW
75	Close Caption Even Field Byte 1	00	RW
76	Close Caption Even Field Byte 2	00	RW
77	Close Caption Odd Field Byte 1	00	RW
78	Close Caption Odd Field Byte 2	00	RW
79	Close Caption Amplitude	00	RW
7A	Close Caption Slope	00	RW
7B	Signature Value 0	00	RO
7C	Signature Value 1	00	RO
7D	Signature Value 2	00	RO
7E	Signature Value 3	00	RO
7F	Signature Value 4	00	RO
80	Signature Value 5	00	RO
81	Signature Value 6	00	RO
82	Signature Value 7 and Close Caption Status	00	RO

Register Descriptions

Offset 00 – Input Selection (00h) ..... RW

7 HDTV Input ..... HDTV_IN
- 0 Disable ..... default
- 1 Enable

6 Interlace Input Mode ..... ITL_IN
- 0 Disable ..... default
- 1 Enable

5 Input Data Y Shift 16 ..... YSH16
- 0 Disable ..... default
- 1 Enable

4 Input Data Cr and Cb Shift 128 ..... CSH128
- 0 Disable ..... default
- 1 Enable

3-0 Input Data Format ..... IDF
- 0000 16-bit /15-bit non-multiplexed RGB input (16-bit /15-bit color) ..... default
- 0001 18-bit non-multiplexed RGB input
- 0010 30-bit multiplexed RGB (30-bit color) input
- 0011 24-bit multiplexed RGB (24-bit color) input
- 0100 24-bit /16-bit multiplexed RGB input (24-bit /16-bit color)
- 0101 15-bit multiplexed RGB input
- 0110 8-bit non-multiplexed YCbCr 422 input
- 0111 10-bit non-multiplexed YcbCr 422 input
- 1000 10-bit / 8-bit multiplexed YCbCr 422 input
- 1001 10-bit multiplexed YCrCb 444 input
- 1010 8-bit multiplexed YCrCb 422 input type I
- 1011 8-bit multiplexed YCrCb 422 input type II
- 1100 8-bit multiplexed YCrCb 422 input type III
- 11xx -reserved-

Offset 01 – Sync Selection 0 (00h) ..... RW

7 TV Vertical Sync Output Polarity ..... VSOP
- 0 Active Low ..... default
- 1 Active High

6 TV Blank Enable ..... BLANK_EN
- 0 Disable ..... default
- 1 Enable

5 TV Blank Input Polarity ..... BLANKP
- 0 Active High ..... default
- 1 Active Low

4 Detect Embedded Sync ..... DES
- 0 Do not detect ..... default
- 1 Sync will be detected from the embedded codes on the pixel input stream

3 Graphic Vertical Sync Direction ..... VSYO
- 0 Input ..... default
- 1 Output – Vsync will be output from encoder chip to graphic chip.

2 Graphic Horizontal Sync Direction ..... HSYO
- 0 Input ..... default
- 1 Output – Hsync will be output from encoder chip to graphic chip.

1 Vertical Sync Polarity ..... VSP
- 0 Active Low ..... default
- 1 Active High

0 Horizontal Sync Polarity ..... HSP
- 0 Active Low ..... default
- 1 Active High

Offset 02 – Sync Selection 1 (00h).....RW

7 CHO Pin Enable ..... CHO_EN
- 0 Disable .....default
- 1 Enable – TV Composite Sync or Hsync

6 CHO Pin Polarity..... CHOP
- 0 Active Low .....default
- 1 Active high

5 CHO Output Pin Select.....CHO
- 0 Output for HSO (TV Horizontal Sync)..default
- 1 Output for CSO (TV Composite Sync)

4 Field Output Enable .....FO_EN
- 0 Disable .....default
- 1 Enable

3 Field Output Polarity .....FOP
- 0 Odd Field Output .....default
- 1 Even Field Output

2 Sync on PB and Pr..... SYNC_PB_PR
- 0 Disable .....default
- 1 Enable

1 Sync on G .....SYNC_G
- 0 Disable .....default
- 1 Enable

0 Sync on B and R..... SYNC_B_R
- 0 Disable .....default
- 1 Enable

Offset 03 –Filter Selection (00h) .....RW

7 Big Edge Filter ..... IN_BLUR
- 0 Disable .....default
- 1 Enable

6 Bypass Progressive Filter.....P_FIL_PASS
- 0 Disable .....default
- 1 Enable

5 Bypass Chroma Filter ..... C_FIL_PASS
- 0 Disable .....default
- 1 Enable

4 Bypass Luma Filter ..... Y_FIL_PASS
- 0 Disable .....default
- 1 Enable

3-2 Adjust Deflicker for Chrominance.....DFK_FC
- 00 No Deflicker Filter.....default
- 01 1:6:1 Deflicker Filter
- 10 1:2:1 Deflicker Filter
- 11 1:1:1 Deflicker Filter

1-0 Adjust Deflicker for Luminance.....DFK_FY
- 00 No Deflicker Filter.....default
- 01 1:6:1 Deflicker Filter
- 10 1:2:1 Deflicker Filter
- 11 1:1:1 Deflicker Filter

Offset 04 – Output Mode (00h) ..... RW

7 HDTV Output..... HDTV_EN
- 0 Disable..... default
- 1 Enable

6 Combinational PAL N Mode .....PAL_NC
- 0 Disable..... default
- 1 Enable (Bit[1:0] must be 11b)

5 PAL_N Mode..... PAL_N
- 0 Disable..... default
- 1 Enable (Bit[1:0] must be 11b)

4 Output Mode ..... OUT_MODE
- 0 Interlace..... default
- 1 Progressive

3-1 Output Line Selection ..... LINE_SEL
- 000 525
- 001 625
- 010 750
- 011 1125
- 1xx -reserved-

0 Output TV Standard..... VOS
- 0 NTSC ..... default
- 1 PAL

Offset 05 – Clock Control (00h) ..... RW

7 XCLK Input Clock Mode ..... XCM
- 0 1x ..... default
- 1 2x

6 POUT Polarity ..... P-OUTP
- 0 Normal ..... default
- 1 Inverted

5 HDTV Non-oversampling Mode HD1XMODE
- 0 Disable ..... default
- 1 Enable

4 Latch Input Data ..... MCP
- 0 Normal clock input ..... default
- 1 Inverted clock input

3-0 Input Clock Adjust ..... DPA
- 0000 Shortest input clock delay ..... default
- …
- 1111 Longest input clock delay

Each increment of this field is one AND gate delay

Offset 06 – Overflow (00h) ..... RW

7-4 Start Active Video Overflow Bits ..... SAV[11:8]

3-0 Horizontal Position Overflow Bits ..... HP[11:8]

Offset 07 – Start Active Video (00h) ..... RW

7-0 Start Active Video Bits 7-0 ..... SAV[7:0]

Sets the delay from the leading edge of horizontal sync to the start of active video

Offset 08 –Start Horizontal Position (00h) ..... RW

7-0 Start Horizontal Position Bits 7-0 ..... HP[7:0]

Used to shift the displayed TV image in a horizontal direction

Offset 09 – Start Vertical Position (00h) ..... RW

7-0 Start Vertical Position Bits 7-0 ..... VP[7:0]

Used to shift the displayed TV image in a vertical direction

Offset 0A – Cr Amplitude Factor (00h) ..... RW

7-0 Cr Amplitude Factor ..... VAMP

Offset 0B – Black Level (00h) ..... RW

7-0 Black Level ..... BLACK_LEVEL

Offset 0C –Y Amplitude Factor (00h) ..... RW

7-0 Luma Amplitude Factor ..... YAMP

Offset 0D – Cb Amplitude Factor (00h) ..... RW

7-0 Cb Amplitude Factor ..... UAMP

Offset 0E – Power Management (00h) ..... RW

7 IO Pad Power Down ..... PWRIO_E
- 0 Disable (IO Pad On) ..... default
- 1 Enable (IO Pad Off)

6 PLL Power Down ..... PWRPLL_E
- 0 Disable (PLL On) ..... default
- 1 Enable (PLL Off)

5 DAC A Power Down ..... PWRA_E
- 0 Disable (DAC A On) ..... default
- 1 Enable (DAC A Off)

4 DAC B Power Down ..... PWRB_E
- 0 Disable (DAC B On) ..... default
- 1 Enable (DAC B Off)

3 DAC C Power Down ..... PWRC_E
- 0 Disable (DAC C On) ..... default
- 1 Enable (DAC C Off)

2 DAC D Power Down ..... PWRD_E
- 0 Disable (DAC D On) ..... default
- 1 Enable (DAC D Off)

1 DAC E Power Down ..... PWRE_E
- 0 Disable (DAC E On) ..... default
- 1 Enable (DAC E Off)

0 DAC F Power Down ..... PWRF_E
- 0 Disable (DAC F On) ..... default
- 1 Enable (DAC F Off)

Offset 0F – Status (00h) ..... RO

7 Macrovision Copy Protection (RO) ..... MACRV

6 Auto correction status ..... AUTO_CR

5 DAC A Status ..... AST

When the output port connects to the monitor and SENSE is in active low level, AST will be set to low level.

4 DAC B Status ..... BST

When the output port connects to the monitor and SENSE is in active low level, BST will be set to low level.

3 DAC C Status ..... CST

When the output port connects to the monitor and SENSE is in active low level, CST will be set to low level.

2 DAC D Status ..... DST

When the output port connects to the monitor and SENSE is in active low level, DST will be set to low level.

1 DAC E Status ..... EST

When the output port connects to the monitor and SENSE is in active low level, EST will be set to low level.

0 DAC F Status ..... FST

When the output port connects to the monitor and SENSE is in active low level, FST will be set to low level.

Offset 10 – Hue Adjustment (00h) ..... **RW**

7-0 **Hue Adjust Bits 7-0** ..... **UE_ADJ[7:0]**
(see Rx11[2:0] for bits 10:8) ..... default = 00

Offset 11 – Overflow and Misc (00h) ..... **RW**

7 **VCO Select Control Bit** ..... **VCN**
6-4 **Change Pump Current Control Bits** ..... **CHC**
3 **Dot Crawl** ..... **DOT_CRAWL**
0 Enable ..... default
1 Disable
2-0 **Hue Adjust Bits 10-8** ..... **HUE_ADJ[10:8]**
(see Rx10 for bits 7:0) ..... default = 00

Offset 12 – PLL P2 Value (00h) ..... **RW**

7-5 **Resister Control Bits** ..... **R**
4-0 **Second Post Divider Control** **P2**

Offset 13 – PLL D Value (00h) ..... **RW**

7-6 **Reserved** ..... always reads 0
5-0 **Pre-Divider Control** ..... **D**

Offset 14 – PLL N Value (00h) ..... **RW**

7-0 **VCO Output Division Factor Bits 7-0** ..... **N[7:0]**
(see Rx15[1:0] for bits 9:8) ..... default = 00

Offset 15 – PLL Overflow(00h) ..... **RW**

7 **Slave or Master Clock Mode** ..... **M_S_REF**
0 Master ..... default
1 Slave
6-2 **First Post Divider Control** ..... **P**
1-0 **VCO Output Division Factor [9:8]** ..... **N[9:8]**
(see Rx14 for bits 7:0) ..... default = 00b
N[9:8] defines the division factor applied to the VCO output.

Offset 16 – Sub-Carrier Value 0 (00h) ..... **RW**

7-0 **Sub-Carrier Value Bits 7:0** ..... **FSCI[7:0]**

Offset 17 – Sub-Carrier Value 1 (00h) ..... **RW**

7-0 **Sub-Carrier Value Bits 15:8** ..... **FSCI[15:8]**

Offset 18 – Sub-Carrier Value 2 (00h) ..... **RW**

7-0 **Sub-Carrier Value Bits 23:16** ..... **FSCI[23:16]**

Offset 19 – Sub-Carrier Value 3 (00h) ..... **RW**

7-0 **Sub-Carrier Value Bits 31:24** ..... **FSCI[31:24]**

Offset 1B – Version ID (50h) ..... **RO**

7-0 **Version ID** ..... **VID**

Offset 1C – Overflow (00h) ..... **RW**

7 **DAC Sense** ..... **SENSE_EN**
0 Disable ..... default
1 Enable
6 **DAC Auto Sense** ..... **AUTO_SENSE**
0 Disable ..... default
1 Enable
5 **TV Mode** ..... **MODE_TV_ENB**
0 Normal TV Function
1 CRT DAC
4 **FSCI Adjust** ..... **FSCI_ADJ**
0 Disable ..... default
1 Enable
3-1 **Start Vertical Position Bit 10-8** ..... **VP[10:8]**
0 **Frequency Conversion Parameter** ..... **K0[8]**

Offset 1D – Testing 0 (00h)..... RW

7 Software Reset
- 0 Reset .....default
- 1 Normal

6-4 Test Mode ..... TS_MD
- 000 Normal
- 001 Function Test
- 010 BIST (Detail)
- 011 BIST (Rough)
- 10x DAC test mode 0 (PD[9:0] for 6 DAC input data, PD[10] for 4 DAC SENSE_ENB input, and PD[17:12] for FST, EST, DST, CST, BST, and AST output))
- 11x DAC test mode 1 (PD[7:0] for DACA and DACC input data, and PD[15:8] for DACB and DACD input data

3 TN_CK ..... TN_CK

2 TS_NAD ..... TS_NAD

1 TS_I2C ..... TS_I2C

Offset 1E – Testing 1 (00h)..... RW

7 Signature ..... SIG_EN
- 0 Off .....default
- 1 On

6-4 Buffer Clock Output Selection ..... BCO_MUX
- 000 Oscillator clock
- 001 External clock after DPA
- 010 Pixel clock
- 011 TV clock
- 100 TV Vsync
- 1xx -reserved-

3 PD[13:12] Output ..... PD[13:12]
- 0 Disable .....default
- 1 Enable

2 PD[11:10] Output ..... PD[11:10]
- 0 Disable .....default
- 1 Enable

1 PD[9:8] Output ..... PD[9:8]
- 0 Disable .....default
- 1 Enable

0 PD[7:0] Output ..... PD[7:0]
- 0 Disable .....default
- 1 Enable

Offset 1F – Filter Switch (00h)..... RW

7-5 Composite Sharpness Cross Color Filter Switch ..... YBW

4-2 Composite Chrominance Cross Luminance Filter Switch ..... CBW

1-2 Other Output Chrominance Cross Luminance Filter Switch .....PBW

Offset 20 – TV Sync Step (00h) ..... RW

7-0 TV Sync Step ..... SYNC_STEP
(see TV Overflow Rx24[0] for bit-8).....default = 00
8-bit step value to control the shape / slope of the sync.

Offset 21 – TV Burst Envelope Step (00h) ..... RW

7-0 TV Burst Envelope Step ..... BURST_STEP
(see TV Overflow Rx24[1] for bit-8).....default = 00
8-bit step value to control the shape / slope of the burst.

Offset 22 – TV Sub-Carrier Phase Adjust ..... RW

7-0 TV Sub-Carrier Phase Adjust..... PHASE_ADJ
(see Rx24[4:2] for bits 10:8).....default = 00
8-bit step value to control the shape / slope of the burst.

Offset 23 – TV Blank Level ..... RW

7-0 TV Blank Level.....BLANK_LEVEL
(see Rx24[5] for bit-8) .....default = 00
8-bit step value to control the base level of the blank signal.

Offset 24 – TV Signal Overflow ..... RW

7-6 Reserved .....always reads 0

5 Bit[8] of TV Blank Level (Rx23).....default = 0

4-2 Bit[10:8] of Sub-Carrier Phase Adjust (Rx22) .....default = 0

1 Bit[8] of TV Burst Envelope Step (Rx21) .....default = 0

0 Bit[8] of TV Sync Step (Rx20).....default = 0

Offset 4A – DAC A/B/C/D Selection (00h).....RW

7-6 DACD Selection .....DACD_SEL
- 00 CVBS
- 01 S-Video 2 C
- 10 RGB 2 G
- 11 Component 2 Y (recommended)

5-4 DACC Selection .....DACC_SEL
- 00 CVBS (recommended)
- 01 S-Video 2 Y
- 10 RGB 1 B
- 11 Component 1 CB (PB)

3-2 DACB Selection.....DACB_SEL
- 00 CVBS
- 01 S-Video 1 C (recommended)
- 10 RGB 1 R
- 11 Component 1 CR (PR)

1-0 DACA Selection .....DACA_SEL
- 00 CVBS
- 01 S-Video 1 Y (recommended)
- 10 RGB 1 G
- 11 Component 1 Y

Offset 4B – DACE and DACF Selection (00h) .....RW

7 Auto Correction Mode Enable ..... AUTO_CR

6 GPO0 Enable .....GPO0_EN
- 0 Disable .....default
- 1 Enable

5 GPO1 Enable .....GPO1_EN
- 0 Disable .....default
- 1 Enable

4 GPO2 Enable .....GPO2_EN
- 0 Disable .....default
- 1 Enable

3-2 DACF Selection.....DACF_SEL
- 00 CVBS
- 01 S-Video 3 Y
- 10 RGB 2 B
- 11 Component 2 CB (PB) (recommended)

..... default = 0000b

1-0 DACE Selection.....DACE_SEL
- 00 CVBS
- 01 S-Video 3 C
- 10 RGB 2 R
- 11 Component 2 CR (PR) (recommended)

Offset 4C – GPO, Coring Function and Undershoot.....RW

7 Reserved

6 General Purpose Output 0 Data.....GPO0_DAT

5 General Purpose Output 1 Data.....GPO1_DAT

4 General Purpose Output 2 Data.....GPO2_DAT

3 Undershoot Check ..... UF_CHK
- 0 Disable .....default
- 1 Enable

2-0 Coring Function Selection..... COR_SEL

Offset 4D – Internal Color Bar and Luma Delay ..... RW

7 Internal CB_EN through Scaler .... FRNT_CB_EN

6 Internal CB_EN on Encoder..... TVOUT_CB_EN

5-4 Internal Color Bar Type..... CB_TYPE

3 Reserved.....always reads 0

2-0 Y Delay Depth ..... Y_DELAY

Offset 4E – UV Delay Control (00h) ..... RW

7 Burst Max Amplitude Bit-8..... BURST_AMP[8]
(see Rx4F for bits 7:0) .....default = 0

6-4 U Delay Depth ..... U_DELAY
- 000 Shortest input clock delay ..... default
- … …
- 111 Longest input clock delay – Each increment of this field is one clock cycle

3 Reserved.....always reads 0

2-0 V Delay Depth ..... V_DELAY
- 000 Shortest input clock delay ..... default
- … …
- 111 Longest input clock delay – Each increment of this field is one clock cycle

Offset 4F – Burst Maximum Amplitude..... RW

7-0 Burst Maximum Value .....BURST_AMP[7:0]
(see Rx4E[7] for bit-8).....default = 00

Offset 50 – Graphic Horizontal Total Pixels..... RW

7-0 Graphic Horiz Total Pixels..... GH_TOTAL[7:0]
(see Rx52[3:0] for bits 11:8).....default = 00

Offset 51 – Graphic Horizontal Active Pixels ..... RW

7-0 Graphic Horiz Active Pixels.....GH_ACTIVE[7:0]
(see Rx52[7:4] for bits 11:8).....default = 00

Offset 52 – Graphic Horizontal Overflow..... RW

7-4 Gr Active Pixels Overflow.....GH_ACTIVE[11:8]
(see Rx51 for bits 7:0).....default = 00

3-0 Gr Total Pixels Overflow..... GH_TOTAL[11:8]
(see Rx50 for bits 7:0).....default = 00

Offset 53 – Graphic Vertical Total Lines ..... RW

7-0 Graphic Vert Total Lines ..... GV_TOTAL[7:0]
(see Rx54[3:0] for bits 10:8).....default = 00

Offset 54 – Graphic Vertical Overflow (00h)..... RW

7 Clock Fast Mode..... F_MODE

6 Adjust XCLK 2X Input Mode .....ADJ_2X

5 TV Clock Fix to 27Mhz ..... TV_FIX_EN

4 Input YCbCr 709 .....EN709

3-0 Gr V Total Lines Overflow..... GV_TOTAL[10:8]
(see Rx53 for bits 7:0).....default = 00

Offset 55 – TV Horizontal Total Pixels ..... RW

7-0 TV Horiz Total Pixels ..... TH_TOTAL[7:0]
(see Rx58[3:0] for bits 11:8) ..... default = 00

Offset 56 – TV Horizontal Active Pixels ..... RW

7-0 TV Horiz Active Pixels ..... TH_ACTIVE[7:0]
(see Rx58[7:4] for bits 11:8) ..... default = 00

Offset 57 – TV Horizontal Sync Width ..... RW

7-0 TV Horiz Sync Width ..... THSYNC_WIDTH [7:0]

Offset 58 – TV Horizontal Overflow ..... RW

7-4 TV Active Pixels ..... TH_ACTIVE[11:8]
(see Rx56 for bits 7:0) ..... default = 00b
3-0 TV Total Pixels ..... TH_TOTAL[11:8]
(see Rx55 for bits 7:0) ..... default = 000b

Offset 59 – TV Burst and TV Broad Pulse Start ..... RW

7-0 TV Burst or Broad Pulse Start .... TB_START[7:0]
(start point from the analog HSYNC falling edge)

Offset 5A – TV Burst and TV Broad Pulse End ..... RW

7-0 TV Burst or Broad Pulse End ..... TB_END[7:0]
(end point from the analog HSYNC falling edge)

Offset 5B – TV Video Start Point ..... RW

7-0 TV Video Start ..... TVIDEO_START[7:0]
(see Rx5D[4] for bit-8) ..... default = 00
(number of pixels between leading edge of analog HSYNC and active video)

Offset 5C – TV Video End Point ..... RW

7-0 TV Video End ..... TVIDEO_END[7:0]
(see Rx5D[5] for bit 12) ..... default = 00
(see Rx5D[3:0] for bits 11:8) ..... default = 00
(number of pixels between leading edge of analog HSYNC and video end)

Offset 5D – TV Video Overflow ..... RW

7 Reserved ..... always reads 0
6 TV Burst End Overflow ..... TB_END[8]
(see Rx5A for bits 7:0) ..... default = 0
5 TV Video End Overflow ..... TVIDEO_END[12]
(see Rx5C for bits 7:0) ..... default = 0
4 TV Video Start Overflow ..... TVIDEO_START[8]
(see Rx5B for bits 7:0) ..... default = 0
3-0 TV Video End Overflow ..... TVIDEO_END[11:8]
(see Rx5C for bits 7:0) ..... default = 00

Offset 5E – Vertical Scale Factor ..... RW

7-0 Vertical Scale Factor ..... VSCALE_FAC[7:0]
(see Rx60 for bits 15:8) ..... default = 00

Offset 5F – Horizontal Scale Factor ..... RW

7-0 Horizontal Scale Factor ..... HSCALE_FAC[7:0]
(see Rx61 for bits 15:8) ..... default = 00

Offset 60 – Scaling Overflow ..... RW

7-0 Vertical Scale Factor ..... VSCALE_FAC[15:8]
(see Rx5E for bits 7:0) ..... default = 00

Offset 61 – Horizontal Blur and Scaling Overflow ..... RW

7-6 Horizontal Scale Filter Enable ..... HSCL_FIL_EN
00 No Filter
01 121
10 11
11 12221
5-4 Reserved
3-0 Horizontal Scale Factor ..... HSCALE_FAC[11:8]
(see Rx5F for bits 7:0) ..... default = 00

Offset 62 – Adaptive Deflicker Length and En Signal .. RW

7-2 Deflicker Threadhold ..... DFK_THD
1-0 Deflicker Type 00 ..... DFK_TYPE
00 Normal
01 Adaptive

Offset 63 – Scaling Horizontal Total Pixels ..... RW

7-0 Scaling Horiz Total Pixels ..... SH_TOTAL[7:0]
(see Rx64[3:0] for bits 11:8) ..... default = 00

Offset 64 – Scaling Horizontal Total Pixels Overflow ... RW

7-4 TV Burst End Overflow ..... TB_END[12:9]
(see Rx5A for bits 7:0, Rx5D[6] for bit 8). default = 0
3-0 Scaling Horiz Total Pixels ..... SH_TOTAL[11:8]
(see Rx63 for bits 7:0) ..... default = 00

Offset 65 – PY Amplitude Factor ..... RW

7-0 PY Amplitude Factor ..... PYAF

Offset 66 – PB Amplitude Factor ..... RW

7-0 PB Amplitude Factor..... PBAF

Offset 67 – PR Amplitude Factor ..... RW

7-0 PR Amplitude Factor ..... PRAF

Offset 68 – Post Divider ..... RW

7-4 Divide the PLL P2 from 1~16 .....POST_DIV_P2

3-0 Divide the PLL P from 1~16 .....POST_DIV_P

Offset 69 –Auto Correction Mode Sense Data ..... RW

7-0 Auto correction mode sense data ...SENSE_DATA
(see Rx6A[1:0] for bits 9:8)

Offset 6A –Field Adjust ..... RW

7-4 Field out adjustment..... FLD_ADJ
Number of lines delays

3-2 Field Type ..... FLD_TYPE
00 Vsync coincides with Hsync in even field
01 Vsync does not coincide with Hsync in even field
10 Reserved
11 Disregard relation between Vsync and Hsync

1-0 Auto correction mode sense data..... ..... SENSE_DATA[9:8]
(see Rx69 for bits 7:0)

Offset 6B –Wide Screen Signal Start Pixel ..... RW

7-0 Wide Screen Signal Start Pixel..... WSS_START
(see Rx6E[5:4] for bits 9:8)..... default = 00

Offset 6C – Wide Screen Signal Data 0..... RW

7-0 Wide Screen Signal Data..... WSS_DATA[7:0]
(see Rx6D for bits 15:8) ..... default = 00
(see Rx6E[3:0] for bits 19:16)..... default = 00

Offset 6D – Wide Screen Signal Data 1..... RW

7-0 Wide Screen Signal Data..... WSS_DATA[15:8]
(see Rx6C for bits 7:0)..... default = 00
(see Rx6E[3:0] for bits 19:16)..... default = 00

Offset 6E – WSS Start and Data Overflow..... RW

7-6 Close Caption Start Pixel..... CC_START[9:8]
(see Rx74 for bits 7:0) ..... default = 00

5-4 Wide Screen Signal Start Pixel. WSS_START[9:8]
(see Rx6B for bits 7:0)..... default = 00

3-0 Wide Screen Signal Data..... WSS_DATA[19:16]
(see Rx6C for bits 7:0)..... default = 00
(see Rx6D for bits 15:8) ..... default = 00

Offset 6F – WSS Sub Carrier Value 0..... RW

7-0 Wide Screen Signal FSCI Value... WSS_FSCI[7:0]
(see Rx70 for bits 15:8) ..... default = 00
(see Rx71[3:0] for bits 19:16) ..... default = 00

Offset 70 – WSS Sub Carrier Value 1 ..... RW

7-0 Wide Screen Signal FSCI Value .WSS_FSCI[15:8]
(see Rx6F for bits 7:0) ..... default = 00
(see Rx71[3:0] for bits 19:16)..... default = 00

Offset 71 – WSS Sub Carrier Value 2 ..... RW

7 Sense Interrupt Enable..... INT_EN
0 Disable..... default
1 Enable

6 Interrupt Status..... INT_ST
0 Disable..... default
1 Enable

5 Interrupt Polarity..... INT_P
0 Active High ..... default
1 Active Low

4 CCIR656 output Enable
0 Disable..... default
1 Enable
(CCIR656 will output through PD12 ~ PD19)

3-0 Wide Screen Signal FSCI ValueWSS_FSCI[19:16]
(see Rx6F for bits 7:0) ..... default = 00
(see Rx70 for bits 15:8)..... default = 00

Offset 72 – Wide Screen Signal Amplitude ..... RW

7-0 Wide Screen Signal Amplitude ..... WSS_AMP[7:0]

Offset 73 – WSS and Close Caption Control Bits..... RW

7-6 Reserved.....always reads 0

5 Enable WSS in Odd Field (525) ..... EN_WSS_F2

4 Enable WSS in Even Field..... EN_WSS_F1

3 Reserved.....always reads 0

2 Close Caption Encoding ..... CC_ENCODE
0 Normal close caption encoding
1 Encode caption when new data bit is received completely

1 Enable Close Caption in Odd Field ..... EN_CC_F2

0 Enable Close Caption in Even Field ..... EN_CC_F1

Offset 74 – Close Caption Start Pixel ..... RW
7-0 Close Caption Start Pixel ..... CC_START

Offset 75 – Close Caption Even Field Byte 1 ..... RW
7-0 CC Data Byte 1 in Even Field ..... CC_F1_B1[7:0]

Offset 76 – Close Caption Even Field Byte 2 ..... RW
7-0 CC Data Byte 2 in Even Field ..... CC_F1_B2[7:0]

Offset 77 – Close Caption Odd Field Byte 1 ..... RW
7-0 CC Data Byte 1 in Odd Field ..... CC_F2_B1[7:0]

Offset 78 – Close Caption Odd Field Byte 2 ..... RW
7-0 CC Data Byte 2 in Odd Field ..... CC_F2_B2[7:0]

Offset 79 – Close Caption Amplitude ..... RW
7-0 Close Caption Amplitude ..... CC_AMP

Offset 7A – Close Caption Slope ..... RW
7-0 Close Caption Increasing Value .. CC_SLOPE[7:0]

Offset 7B – Signature Value 0 ..... RO
7-0 Signature Output Value ..... SIG_OUT[7:0]

Offset 7C –Signature Value 1 ..... RO
7-0 Signature Output Value ..... SIG_OUT[15:8]

Offset 7D –Signature Value 2 ..... RO
7-0 Signature Output Value ..... SIG_OUT[23:16]

Offset 7E –Signature Value 3 ..... RO
7-0 Signature Output Value ..... SIG_OUT[31:24]

Offset 7F –Signature Value 4 ..... RO
7-0 Signature Output Value ..... SIG_OUT[39:32]

Offset 80 – Signature Value 5 ..... RO
7-0 Signature Output Value ..... SIG_OUT[47:40]

Offset 81 – Signature Value 6 ..... RO
7-0 Signature Output Value ..... SIG_OUT[55:48]

Offset 82 – Signature Value 7 and Close Caption ..... RO
7-6 Reserved ..... always reads 0
5 Close Caption Value ..... CC_STAT_F2
4 Close Caption Value ..... CC_STAT_F1
3-0 Signature Output Value ..... SIG_OUT[59:56]

FUNCTIONAL DESCRIPTIONS

Architecture Description

Data Capture

- Digital RGB 24/30-bit color input video data in both interlace and non-interlace formats with 12/15-bit multiplexed input data path depth
- Digital RGB 15/16/18-bit color input video data in both interlaced and non- interlaced formats with 8-bit multiplexed or 15/16/18-bit non-multiplexed input data path depth
- Digital YCrCb 8/10 or 16/20-bit 4:2:2 (CCIR656, CCIR601) input video format in interlace or non-interlace formats with 16-bit multiplexed or 20-bit non-multiplexed input data path depth.
- Digital YCrCb 8/10 or 16/20-bit 4:2:2 HDTV input video format (BT709, BT1120, SMPTE274M) in both interlace and non-interlace formats with 16-bit multiplexed or 20-bit non-multiplexed input data path depth.
- Digital YCrCb 24/30-bit 4:4:4 color input data in both interlace and non-interlace formats with 12/15-bit multiplexed input data path depth
- Flexible pixel ordering with various alternate formats (Please check next page about the Input Data Format table for more detail)

Color Space Converter

This module converts data capture formats to YUV 422 format or converts the YUV 422 format to RGB format (Scart RGB)

Scaler and Deflicker

This module converts the lines of input pixel data to the appropriate number of output lines for producing a full-screen image on the television receiver. The image can be scaled to 100% within the viewable area of the screen. The device can perform vertical filtering to reduce the effects of picture flicker due to the interlacing of the output image. Because this process trades off vertical resolution in order to reduce flicker, the amount of flicker filtering is programmable and allows the process to be optimized for the specific image. This module generates YUV444 pixel data from the interlaced image to the encoder module.

Encoder

This module accepts the YUV444 pixel data and converts it to a standard baseband television signal that is compatible with worldwide standards including PAL (B, D, G, H, I, N, Nc, M) and NTSC (M, J). The Y data can be manipulated for contrast control and a setup level can be added for brightness control. The U, V data can be scaled to achieve color saturation control. Also, the U, V signals are modulated by the appropriate sub-carrier sine/cosine waveforms and a phase offset may be added onto the color sub-carrier during active video to allow hue adjustment. The resulting U and V signals are added together to make up the chrominance signal. The luma (Y) and chroma signals are added together to make up the composite video signal. Separated luma and chroma signals make up the S-Video signal.

DAC

The VT1625 and VT1625M contain six 10-bit DACs. Each DAC is used to convert digital composite, luma, chroma, RGB, YCbCr data to analog signals, as well as be individually powered off if not required. In addition, the DAC module has an auto-detection circuit, which provides a way to sense the connection of a TV.

Serial Bus Interface

The VT1625 and VT1625M contain a standard serial bus control port through which the control registers can be written and read. The serial bus address is 40h (Low) or 42h (High) depending on the strapping of the ADDR pin level.

CRTC

The VGA controller normally supplies the horizontal and vertical sync signals, however, the chip can also generate the signals. This module generates the horizontal and vertical sync signals. In CCIR656 input mode, the embedded sync may also be used.

PLL

Both of the VT1625 and VT1625M contain a high accuracy, low-jitter phase-locked-loop to create outstanding quality video. Normal operation requires the encoding clock to be generated by the PLL. In master clock mode, the reference clock of the PLL is provided by OSC and the frequency is 27 (± 20 ppm) MHz. In slave clock mode, the reference clock is input via the XCLK pin.

Digital Video Interface

Table 4. Input Data Format

IDF	0 565/555 RGB		1 666 RGB	2 101010 30-bit RGB		3 888 24-bit RGB		4 888/565 24-bit / 16-bit RGB				5 555 15-bit RGB	
Pixel / Pin				P#A	P#B	P#A	P#B	P#A		P#B		P#A	P#B
PD19	X		X	X	X	X	X	X		X		X	X
PD18	X		X	X	X	X	X	X		X		X	X
PD17	X		R5	X	X	X	X	X		X		X	X
PD16	X		R4	X	X	X	X	X		X		X	X
PD15	R4	R4	R3	X	X	X	X	X		X		X	X
PD14	R3	R3	R2	G4	R9	X	X	X		X		X	X
PD13	R2	R2	R1	G3	R8	X	X	X		X		X	X
PD12	R1	R1	R0	G2	R7	X	X	X		X		X	X
PD11	R0	R0	G5	G1	R6	G3	R7	G4	G2	R7	R4	X	X
PD10	G5	G4	G4	G0	R5	G2	R6	G3	G1	R6	R3	X	X
PD9	G4	G3	G3	B9	R4	G1	R5	G2	G0	R5	R2	X	X
PD8	G3	G2	G2	B8	R3	G0	R4	B7	B4	R4	R1	X	X
PD7	G2	G1	G1	B7	R2	B7	R3	B6	B3	R3	R0	G2	X
PD6	G1	G0	G0	B6	R1	B6	R2	B5	B2	G7	G5	G1	R4
PD5	G0	0	B5	B5	R0	B5	R1	B4	B1	G6	G4	G0	R3
PD4	B4	B4	B4	B4	G9	B4	R0	B3	B0	G5	G3	B4	R2
PD3	B3	B3	B3	B3	G8	B3	G7	G0	0	R2	0	B3	R1
PD2	B2	B2	B2	B2	G7	B2	G6	B2	0	R1	0	B2	R0
PD1	B1	B1	B1	B1	G6	B1	G5	B1	0	R0	0	B1	G4
PD0	B0	B0	B0	B0	G5	B0	G4	B0	0	G1	0	B0	G3

IDF	6 8-bit 4:2:2 YCbCr	7 10-bit 4:2:2 YCbCr	8 10-bit / 8-bit 4:2:2 YCbCr				9 10-bit 4:4:4 YCbCr		10 8-bit 4:4:4 YCbCr		11 8-bit 4:4:4 YCbCr		12 8-bit 4:4:4 YCbCr	
Pixel / Pin			P#A		P#B		P#A	P#B	P#A	P#B	P#A	P#B	P#A	P#B
PD19	X	Y9	X		X		X	X	X	X	X	X	X	X
PD18	X	Y8	X		X		X	X	X	X	X	X	X	X
PD17	X	Y7	X		X		X	X	X	X	X	X	X	X
PD16	X	Y6	X		X		X	X	X	X	X	X	X	X
PD15	Y7	Y5	X		X		X	X	X	X	X	X	X	X
PD14	Y6	Y4	X		X		Y4	Cr9	X	X	X	X	X	X
PD13	Y5	Y3	X		X		Y3	Cr8	X	X	X	X	X	X
PD12	Y4	Y2	X		X		Y2	Cr7	X	X	X	X	X	X
PD11	Y3	Y1	X		X		Y1	Cr6	Y3	Cr7	Cr7	Y7	Y4	Cr7
PD10	Y2	Y0	X		X		Y0	Cr5	Y2	Cr6	Cr6	Y6	Y3	Cr6
PD9	Y1	C9	C9	C7	Y9	Y7	Cb9	Cr4	Y1	Cr5	Cr5	Y5	Y2	Cr5
PD8	Y0	C8	C8	C6	Y8	Y6	Cb8	Cr3	Y0	Cr4	Cr4	Y4	Cb7	Cr4
PD7	C7	C7	C7	C5	Y7	Y5	Cb7	Cr2	Cb7	Cr3	Cr3	Y3	Cb6	Cr3
PD6	C6	C6	C6	C4	Y6	Y4	Cb6	Cr1	Cb6	Cr2	Cr2	Y2	Cb5	Y7
PD5	C5	C5	C5	C3	Y5	Y3	Cb5	Cr0	Cb5	Cr1	Cr1	Y1	Cb4	Y6
PD4	C4	C4	C4	C2	Y4	Y2	Cb4	Y9	Cb4	Cr0	Cr0	Y0	Cb3	Y5
PD3	C3	C3	C3	C1	Y3	Y1	Cb3	Y8	Cb3	Y7	Cb7	Cb3	Y0	Cr2
PD2	C2	C2	C2	C0	Y2	Y0	Cb2	Y7	Cb2	Y6	Cb6	Cb2	Cb2	Cr1
PD1	C1	C1	C1	0	Y1	0	Cb1	Y6	Cb1	Y5	Cb5	Cb1	Cb1	Cr0
PD0	C0	C0	C0	0	Y0	0	Cb0	Y5	Cb0	Y4	Cb4	Cb0	Cb0	Y1

Input and Output Resolution

VT1625 and VT1625M can accept input resolution from 640x480 to 1024x768 by graphic controller, also including 1280x720, 1920x1080 HDTV input resolution, and encoder these input resolution to variable TV system resolution. Table 5 shows these configurations.

Table 5. Input / Output Configuration

Input configuration			Output Configuration				
GFX Resolution	Frame (Hz)	RGB / YCrCb	NTSC-480i	PAL-576i	480P / 576p	720p	1080i
640x480~1024x768	59.94p/i 50p/i	*	*	*	*	*	*
1024x768~1920x1080	60p/59.94p/50p	*			*	*	
1920x1080	60p/59.94p/50p						*
1920x1080	60i/59.94i/50i	*					*

"p"- progressive format / frame rate, "i" – interlace format / field rate, 480i / 480p is same as 525i / 525p, 576i / 576p is same as 625i / 625p.

Video DAC output setting

Rx4A and Rx4B for the video DAC output setting

Register setting	DAC A Rx4A[1-0]	DAC B Rx4A[3-2]	DAC C Rx4A[5-4]	DAC D Rx4A[7-6]	DAC E Rx4B[1-0]	DAC F Rx4B[3-2]
00	Composite 1	Composite 2	Composite 3	Composite 4	Composite 5	Composite 6
01	S-Video 1 (Y)	S-Video 1 (C)	S-Video 2 (Y)	S-Video 2 (C)	S-Video 3 (C)	S-Video 3 (Y)
10	RGB 1 (G)	RGB 1 (R)	RGB 1 (B)	RGB 2 (G)	RGB 2 (R)	RGB 2 (B)
11	Component 1 (Y)	Component 1 (Pr)	Component 1 (Pb)	Component 2 (Y)	Component 2 (Pr)	Component 2 (Pb)

Serial Bus Interface

1. VT1625 and VT1625M Register Read / Write Control

VIA VT1625 and VT1625M support serial bus interface. This serial interface consists of two signals: SBD (bidirectional Serial Bus Data) and SBC (Serial Bus Clock). The registers can be write / read through the serial bus. The SBC is input only and driven by the output of the graphic controller device. The SBD can be the input or output of the TV-Encoder depending on the write / read status.

2. Serial Bus Address

VT1625 and VT1625M support two different serial bus addresses: 40H or 42H for selection and determined by the status of the ADDR (address select) pin. Low for 40H and High for 42H.

Device Address Byte (DAB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	0	0	ADDR	R/W

Device Address Byte (DAB) --- 40H (ADDR pin is pulled low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	0	0	0	R/W

Master / Slave Clock Mode

VT1625 and VT1625M can be configured to be in either master or slave clock mode. In master clock mode, it provides the pixel clock signal to the video source and expects incoming data to be available when required. In slave clock mode, the TV encoder chip accepts the external pixel clock from the video source.

Master Mode

In master clock mode, the VT1625 and VT1625M work as a master and the video source device works as a slave. It provides a clock signal through the PCLK pin to the video source device. The video source device will use this clock as a frequency reference. Then the video source will generate a clock signal into the XCLK pin. The TV encoder chip will use this clock signal to latch incoming data. The PCLK clock signal can also be treated as the input clock signal connected directly to the XCLK pin. The HSYNC and VSYNC signals can be programmed to be either input or output to the TV encoder chip. The master clock mode can be configured as mode 1 or mode 2. See illustrations in Figure 3 and Figure 4.

Slave Mode

In slave clock mode, the VT1625 and VT1625M work as a slave and the video source device works as a master. The video source device will generate a clock signal input to the XCLK pin. Through the XCLK pin, it receives a clock from the video source device and uses this clock to latch incoming data. Moreover, this clock will be a reference clock of the TV encoder chip for generating a pixel clock. The HSYNC and VSYNC signals can be programmed to be either input or output to the TV encoder chip. In slave clock mode, the VT1625 and VT1625M can be configured as illustrated in Figure 5.

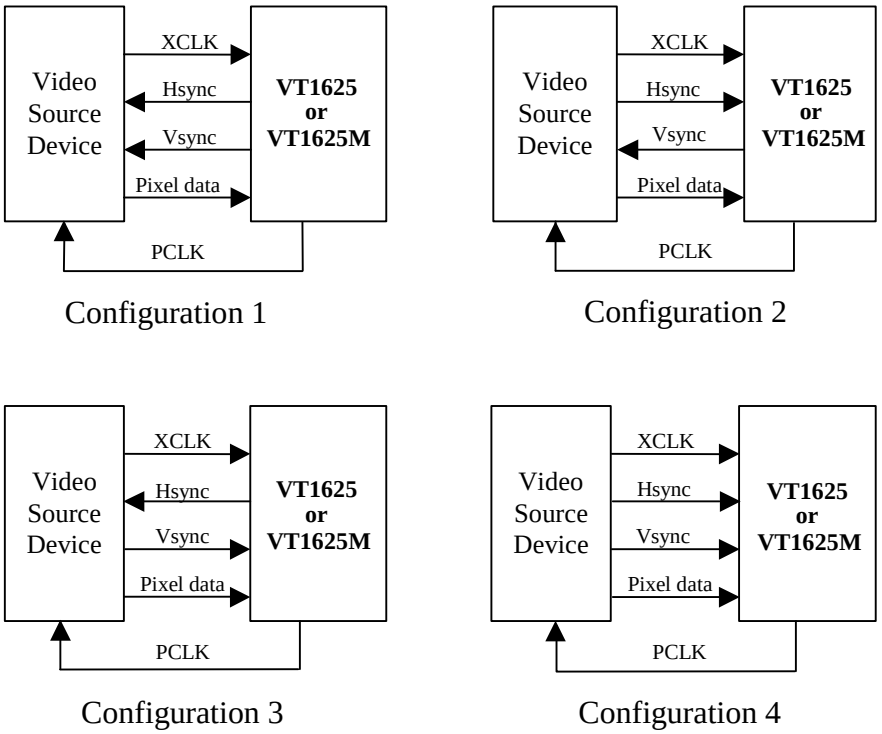


Figure 3. Master Clock Mode 1

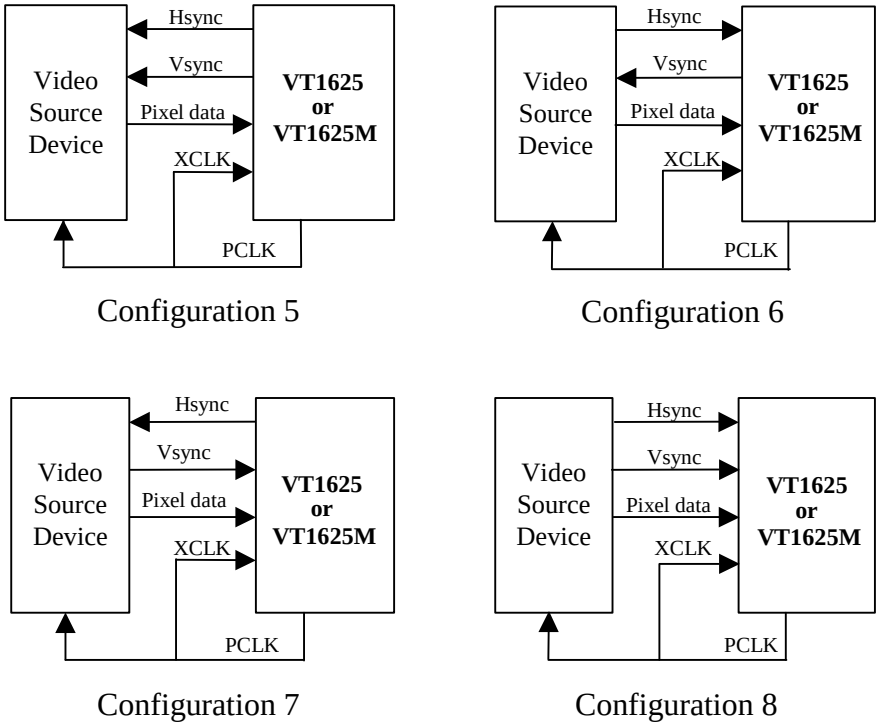


Figure 4. Master Clock Mode 2

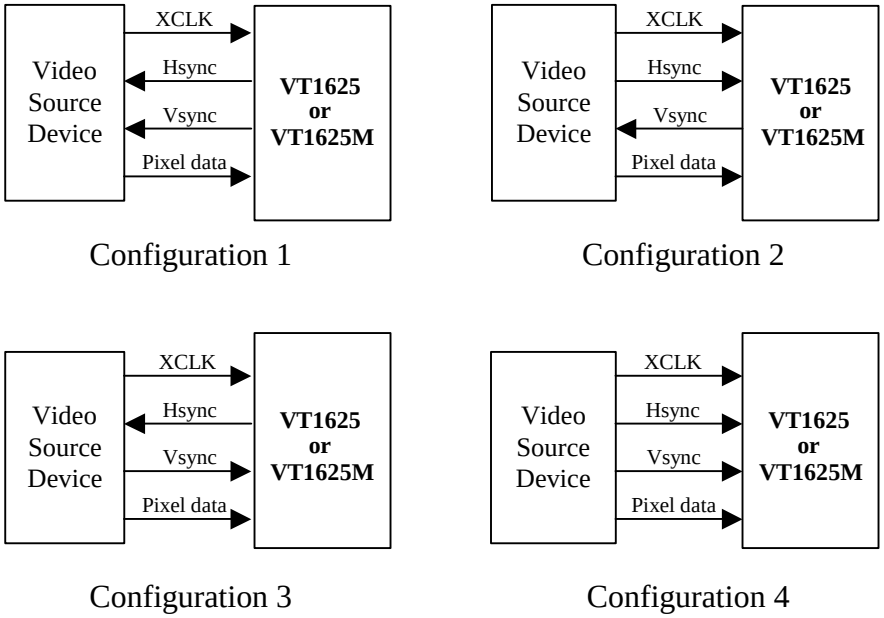


Figure 5. Slave Clock Mode

Color Bar Generator

The VT1625 and VT1625M have a built-in color bar generator that generates the 75% amplitude and 100% saturation EIA colors for the NTSC and PAL standards. They also provide a black screen and a blue screen. While in color bar mode, input pixel data is ignored.

Sub-carrier Generation

The VT1625 and VT1625M use a 32-bit-word to synthesize the sub-carrier. The value of the sub-carrier increment required to generate the desired sub-carrier frequency is found with the following equations:

NTSC: $FSCI[31:0] = 2^{32} * [455 / (2 * H\_Total)]$
-or- $FSCI[31:0] = (int) (2^{32} * 3.579545 / F_{clk})$

PAL: $FSCI[31:0] = 2^{32} * [(1135/4 + 1/625) / (H\_Total)]$
-or- $FSCI[31:0] = (int) (2^{32} * 4.43361875 / F_{clk})$

where H_Total is the number of output pixels per line and F_{clk} is the encoder clock frequency if FSCI_ADJ_EN = 0 and F_{clk} = 27 MHz if FSCI_ADJ_EN = 1. This allows the generation of any desired sub-carrier for any desired video standard. The 32-bit sub-carrier increment FSCI[31:0] must be loaded by the serial interface before the sub-carrier can be enabled. In order to maintain the correct SCH phase and to prevent any residual errors from accumulating, the sub-carrier will automatically adjust to meet the specification.

Burst Generation

Sub-carrier burst generation is a function of the video standard (e.g. NTSC or PAL), the sub-carrier frequency increment (FSCI), and the burst horizontal begin (TB_START) and end (TB_END) register settings. The burst will automatically be blanked during horizontal sync to prevent invalid sync pulses from being generated. Burst blanking is automatically controlled by the selected video format and the BURST_AMP setting can program the burst amplitude.

Tri-Level Synchronization and Broad Pulse Generation

VT1625 and VT1625M will add the tri-level synchronization and broad pulse automatically when it encodes to HDTV output (720p or 1080i). The width of tri-level synchronization is controlled by THSYNC_WIDTH register and the broad pulse is controlled by TB_START and TB_END.

Field output

VT1625 and VT1625M support field output. It is enabled by FO_EN and the polarity can be controlled by FOP. Using FLD_ADJ can delay the field output.

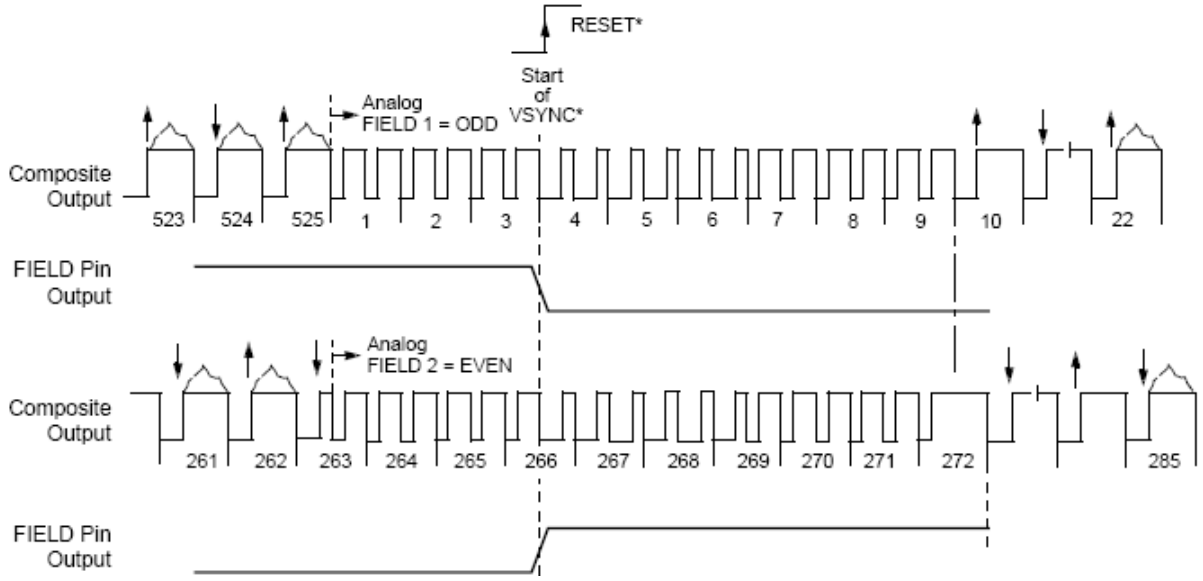


Figure 6. Field Output

Luma and Chroma Processing

Use the YBW, CBW and PBW registers to control the bandwidth of luminance, chrominance and HDTV signal. Use the Y_FIL_PASS, C_FIL_PASS, P_FIL_PASS registers to turn these filters off individually.

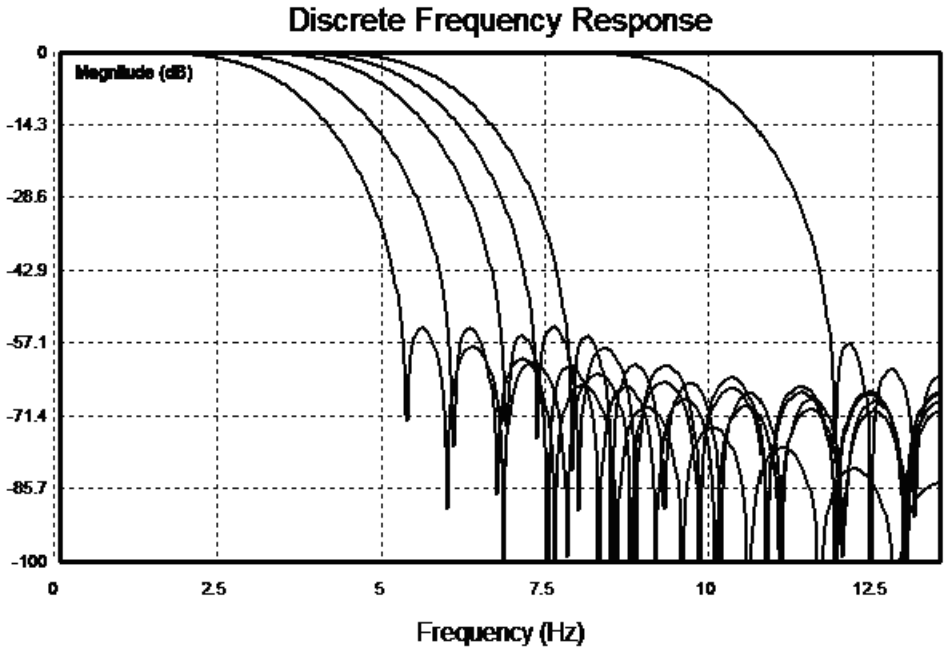


Figure 7. Luma filter

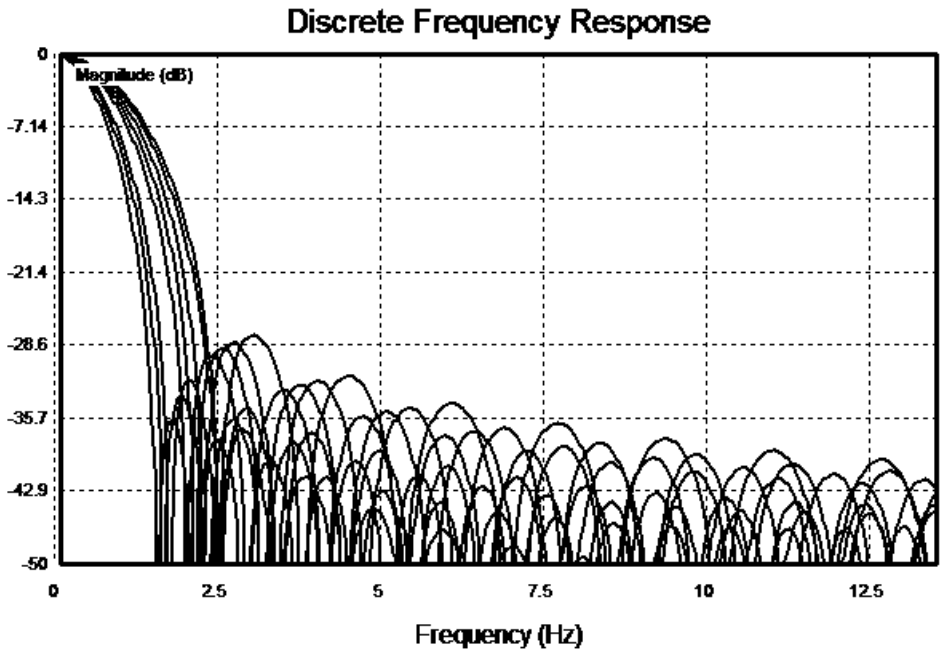


Figure 8. Chroma filter

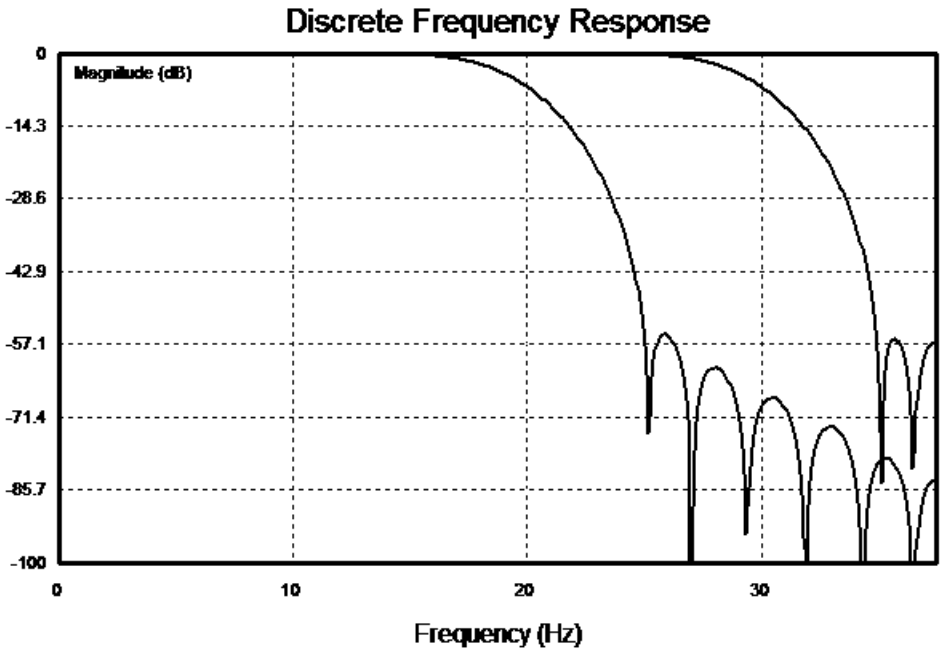


Figure 9. HDTV pass filter

Power Down Mode

The VT1625 and VT1625M can be powered down by programming their registers and each of the DACs can be powered down independently if not used. The PLL and IO pad can be turned off to save more power. All register contents are maintained when the two TV encoder chips are in power down mode.

Macrovision Copy Protection

The VT1625M implements the Macrovision 7.1.L1 copy protection process and Macrovision 1.2 AGC copy protection with 525p / 625p progressive scan output. This process changes the encoded output of the NTSC / PAL signals to inhibit recording on VCR devices while not affecting viewing on a TV. All parameters that control the copy protection process are fully programmable but are not documented in this data sheet per legal requirements of Macrovision Corporation.

Display Modes

The VT1625 and VT1625M are designed to accept any input resolution from 640x480 up to 1024x768 by setting the TV CRTC registers, the scaling registers and the TV timing registers. The TV CRTC registers include the GH_TOTAL, GV_TOTAL, GH_ACTIVE, SH_TOTAL, TH_TOTAL, and TH_ACTIVE register bits. These registers decide the horizontal active and total pixels, total lines for the input data, and the output horizontal active and total pixels for the TV display after scaling. The TV encoder chip is capable of scaling down or up the input images in any size from 1.5 to 0.5 factors in the vertical and horizontal directions by setting the VSCAL_FAC and HSCAL_FAC register bits. The TV encoder chip does not contain a frame memory. Therefore, the output frame rate must be synchronous to the input frame rate. To accomplish this, the input total, output total, scaling ratio, and the pixel frequency must be set to proper values for a corresponding relationship.

Since the pixel frequency varies from every input resolution and the TV timing is fixed, different values must be programmed in the TV timing registers for every input resolution. The TV timing registers include the THSYNC_WIDTH, TBURST_START, TBURST_END, TVIDEO_START, and TVIDEO_END register bits.

Clock Frequency

A crystal must be present between the XI and XO pins for generating a 27 MHz reference clock for the PLL (Phase Lock Loop). In master clock mode, the PLL uses this clock as a reference. In slave clock mode, the PLL uses the clock from the XCLK pin as a reference clock. The PLL generates 2 clocks: One is the pixel clock output on the PCLK pin (for master mode use only) and the other is the pixel clock used by the Encoder engine. The frequency is calculated using the following formula:

$F_{CLK} = [F_{REFCLK} * N / (D*P*(P\_D+1))]$ MHz (P_D means post divider)

$Ftvclk = F_{RefClk} * N/(D*P2*(P\_D2+1))$ MHz (P_D2 means post divider 2)

In master mode:
Fclk = Input Pixel Clock = GH_Total * GV_Total * Vsync
Ftvclk = Fclk (P/P2) = TH_Total*TV_Total*Vsync

TH_Total = (GH_Total / Scaling Ratio)*(P/P2)
TV_Total = 525 (NTSC) or 625 (PAL)
Vsync = 59.94Hz (NTSC) or 50Hz (PAL)

(D, P, and P2 are programmed in increments of 0.5; N and R are programmed in increments of 1.0).

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
T_{STG}	Storage Temperature	–65		150	ºC
T_j	Junction Operating Temperature			125	ºC
T_{AMB}	Ambient Operating Temperature	0		70	ºC
V_I	Input Voltage (all digital pins)	GND – 0.25		VCC+0.25	V
V_{ESD}	Electrostatic Discharge (Human Body)			2	kV
T_{VPS}	Vapor Phase Soldering (1 min.)			220	ºC

Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33	I/O Voltage	3.15	3.3	3.45	V
VCC25	Digital Power Supply Voltage	2.25	2.5	2.75	V
VCCPLL	PLL Power	2.25	2.5	2.75	V
VCCDAC	DAC Power	2.25	2.5	2.75	V
VCCOSC	Oscillator Power	2.25	2.5	2.75	V
VCCBGAP	Band Gap Power	2.25	2.5	2.75	V
R_L	Output load to DAC outputs		37.5		Ω

DC Characteristics and Power Consumption Specification for Different Resolutions

Table 6. Resolution 1024 x 768

Symbol	Parameter	Min	Typ	Max	Unit
ID33	VCC33 (3.3V)		5		mA
ID25	VCC25 (2.5V)		92.2		mA
IPLL	VCCPLL (2.5V)		11.3		mA
IDAC	VCCDAC (2.5V) – All 6 DACs power on		210		mA
IVCCQ	VCCQ (1.5V)		2.6		mA
P Total	Total Power Consumption			0.9	W

Table 7. Resolution 1280 x 720 (HDTV Mode 720p Output)

Symbol	Parameter	Min	Typ	Max	Unit
ID33	VCC33 (3.3V)		5		mA
ID25	VCC25 (2.5V)		135		mA
IPLL	VCCPLL (2.5V)		20		mA
IDAC	VCCDAC (2.5V) – All 6 DACs power on		210		mA
IVCCQ	VCCQ (1.5V)		3.4		mA
P Total	Total Power Consumption			1	W

Table 8. Resolution 1920 x 1080 (HDTV Mode 1080i Output)

Symbol	Parameter	Min	Typ	Max	Unit
ID33	VCC33 (3.3V)		5		mA
ID25	VCC25 (2.5V)		191		mA
IPLL	VCCPLL (2.5V)		22.5		mA
IDAC	VCCDAC (2.5V) – All 6 DACs power on		210		mA
IVCCQ	VCCQ (1.5V)		6.5		mA
P Total	Total Power Consumption			1.1	W

DC Specifications – LVTTL Mode (V_{CCQ} = 3.3V, V_{REF} = 1.65V)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VCC33	I/O voltage	3.0		3.6	V	Normal op.
V_{IL}	Input low voltage	–0.5		0.3 VCC	V	non 5V tolerant
V_{IH}	Input high voltage	0.7 VCC		1.05 VCC	V	non 5V tolerant
V_{IH5T}	Input high voltage	0.7 VCC		5.5 V	V	5V tolerant
V_{OL}	Output low voltage	-		0.1 VCC	V	I_{OL}= 3.2mA
V_{OH}	Output high voltage	0.7 VCC		-	V	I_{OH}= -200mA
I_{OZ}	Input leakage	–10		10	mA	$0 < V_{IN} < VCC$
C_{IN}	Input capacitance	-		10	pF	
C_{OUT}	Output capacitance	-		10	pF	

DC Specifications – Low Swing Input Mode (V_{CCQ} = 1.5V, V_{REF} = 0.75V)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CCQ}	I/O Voltage	1.35		1.65	V	Normal op.
V_{REF}	Low Swing Differential Input Reference Voltage		$1/2V_{CCQ}$		V	
V_{IHLS}	Low Swing High Level Input Voltage	V_{REF}+100mV		1.8	V	
V_{ILLS}	Low Swing Low Level Input Voltage	GND		V_{REF}-100mV	V	

DAC DC Characteristics

Table 9. DAC DC Characteristics

Parameter		Min	Typ	Max	Unit
Full scale Current	TV Mode		34		mA
	CRT Mode		18.7		mA
Output Voltage Range	TV Mode		1.23		V
	CRT Mode		700		mV
DAC Resolution			10		Bits
INL			±1.0		Lsb
DNL			±1.0		Lsb
Gain Error			5		%
DAC to DAC Matching			2		%
RSET Resistor			4.42		KΩ
Output Loading			10		pF
Output Load Resistor			37.5		Ω
Band Gap Reference Voltage			1.22		V
SENSE Reference Voltage	TV Mode		1.22		V
	CRT Mode		0.61		V
Delay Time of SENSE Output			10		ns
Glitch Impulse Energy			75		pV-sec
TV Mode	Power on current (Analog)		220.7		mA
	Power on current (Digital)		12.3		mA
CRT Mode	Power on current (Analog)		121.3		mA
	Power on current (Digital)		12.3		mA
Sleep Current (power down)			20		uA

DAC AC Characteristics

Table 10. DAC AC Characteristics

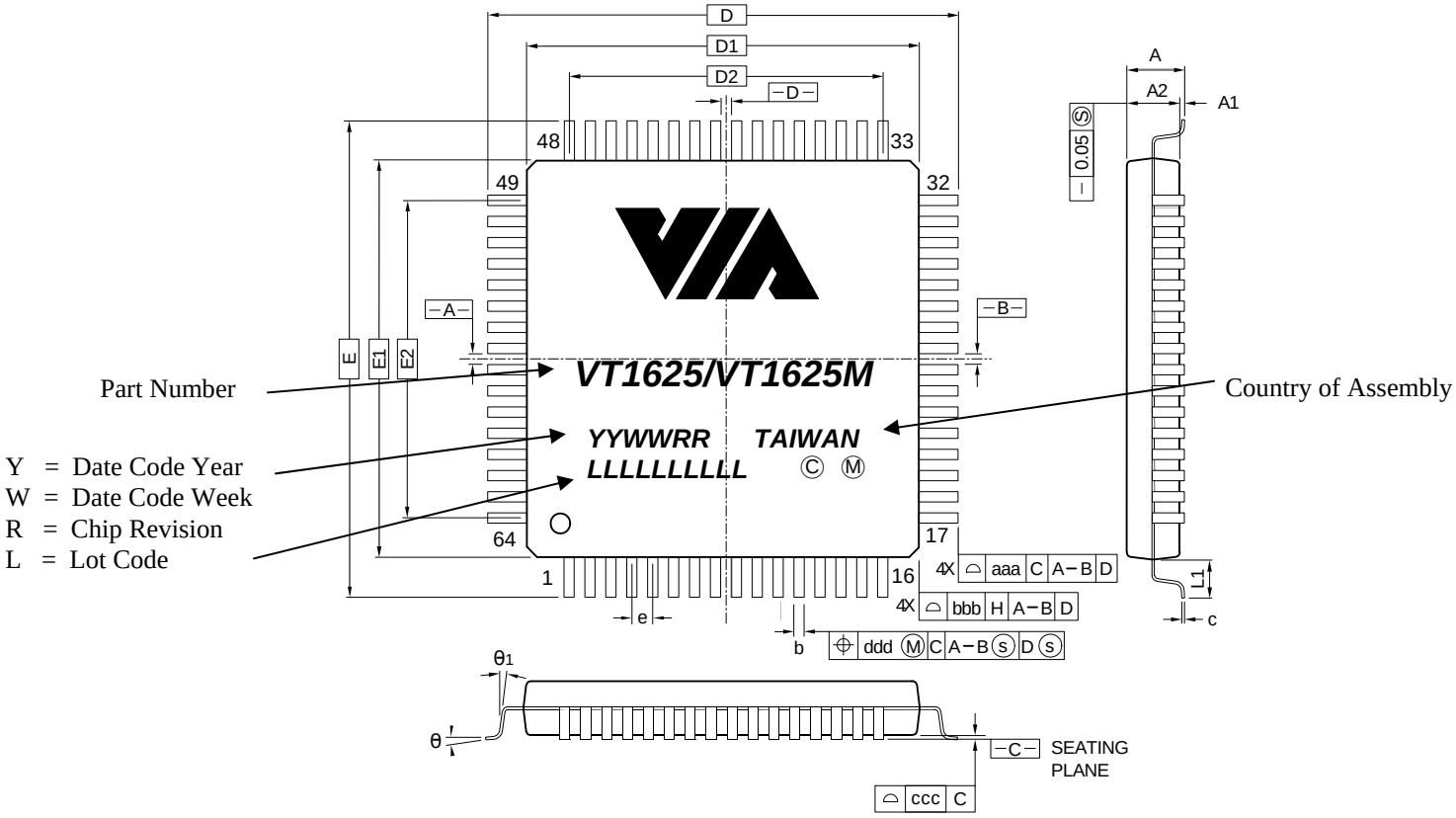
Parameter	Min	Typ	Max	Unit
Frequency		150		MHz
Output Rising Time		2		ns
Output Falling Time		2		ns
Full Scale Settling Time within ±½ LSB		5.8		ns
CLK to valid output		0.5clk+2.1 ns		Tclk
Data Setup Time which samples by CLK		1.0		ns
Data Hold Time which samples by CLK		1.0		ns

PLL Characteristics

Table 11. PLL Characteristics

Parameter	Min	Typ	Max	Unit
Power Supply	2.25		2.75	V
Clock Output Duty Cycle	45		55	%

PACKAGE MECHANICAL SPECIFICATIONS



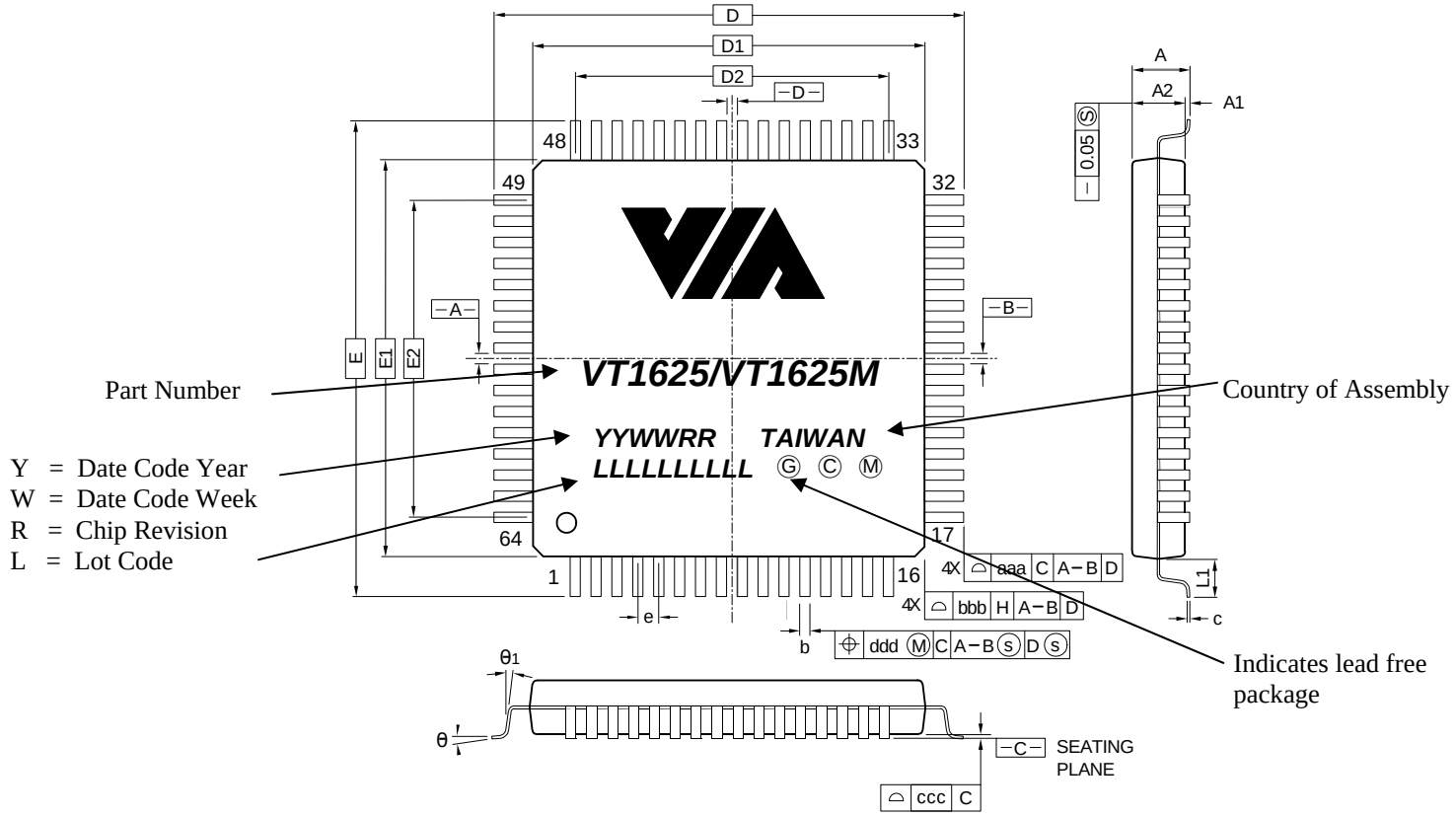
NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	12.00 BASIC			0.472 BASIC		
E	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.393 BASIC		
E1	10.00 BASIC			0.393 BASIC		
D2	7.50 BASIC			0.295 BASIC		
E2	7.50 BASIC			0.295 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ_1	0	—	—	0	—	—
θ_2	11	12	13	11	12	13
θ_3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 10. Mechanical Specification – 64-Pin TQFP Pack



NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	12.00 BASIC			0.472 BASIC		
E	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.393 BASIC		
E1	10.00 BASIC			0.393 BASIC		
D2	7.50 BASIC			0.295 BASIC		
E2	7.50 BASIC			0.295 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 11. Mechanical Specification for Lead-Free – 64-Pin TQFP Pack